Contents of System Module GR8

System Module GR8

Introduction

GR8 is the baseband/RF module NHE–4 cellular tranceiver. The GR8 module carries out all the system and RF functions of the tranceiver. System module GR8 is designed for a handportable phone, that operate in GSM system.

Technical Section

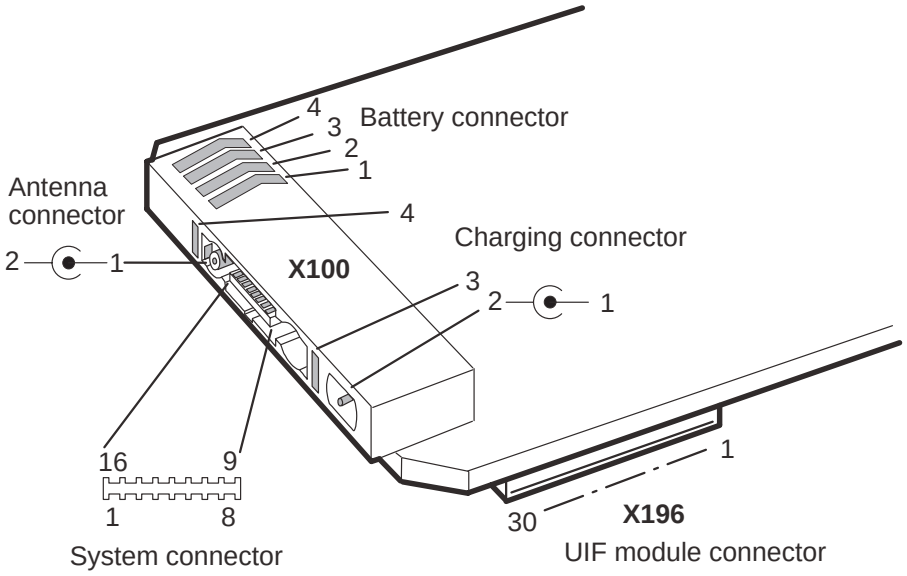
All functional blocks of the system module are mounted on a single multi layer printed circuit board. The chassis of the radio unit has separating walls for baseband and RF. All components of the baseband section are surface mountable. They are soldered using reflow. The connections to accessories are taken through the bottom connector of the radio unit. The connections to the User Interface module (UIF) are fed through a flex connector. There is no physical connector between the RF and baseband sections.

WARNINGS

The maximum battery voltage during the transmission should not exceed 8.0 V. Higher battery voltages may destroy the power amplifier. This will be quaranteed by hardware based limiting which has maximum value 7.6 ±0.3 V.

External and Internal Connectors

The system module has two connector, external bottom connector and internal UIF module connector.



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Bottom Connector X100

System Connector

Pin:	Name:	Description:
1, 9	GND	Digital ground
2	MIC/JCONN	External audio input from accessories or handsfree microphone. Multiplexed with junction box connection control signal. 16.8 kΩ pull down in phone.
3	AGND	Analog ground for accessories. Connected directly to digital ground on the PCB.
4	TDA	Transmitted DBUS data to the accessories.
5	M2BUS	Serial bidirectional data and control between the handportable and accessories.
6	HOOK/RXD2	HOOK indication. The phone has a 100 kΩ pull–up resistor. Data to flash from flash programmer.
7	PHFS/TXD2	Handsfree device power on/off. Data to flash programming device.
8, 16	VCHAR	Battery charging voltage.
10	EAR/HFPWR	External audio output to accessories or handsfree speaker. 100 kΩ pull–down resistor in phone to turn on the junction box.
11	DSYNC	DBUS data bit sync clock.
12	RDA	DBUS received data from the accessories.
13	NC	Not used.
14	VF	Programming voltage for flash.
15	DCLK	DBUS data clock.

Battery Connector

Pin:	Name:	Description:
1	GND	Ground
2	TBAT	Battery temperature
3	BTYPE	Battery type
4	VBATT	Battery voltage

Charging Connector

Pin:	Name:	Description:
1	VCHAR	Battery charging voltage
2	GND	Ground
3	VCHAR	Battery charging voltage
4	GND	Ground

Antenna Connector

Pin:	Name:	Description:
1	RF EXT	External antenna signal
2	GND	Ground

UIF Module Connector X196

Pin:	Name:	Description:
1	VL1	Logic supply voltage 4.65 V
2	GND	Ground
3, 30	VBATT	Battery voltage
4	BACKLIGHT	Backlights on/off
5 – 8	UIF(0;3)	Lines for keyboard read and LCD controller
9	UIF4	Line for keyboard read and LCD controller read/write strobe
10	UIF5	Line for keyboard read and LCD controller data/instruction register selection
11	UIF6	LCD controller enable strobe
12	MIC ENA	Microphone bias enable
13 – 16	COL(0;3)	Lines for keyboard write
17	CALL LED	Call LED enable
18	MICP	Microphone (positive node)
19	MICN	Microphone (negative node)
20	EARP	Earpiece (negative node)
21	EARN	Earpiece (positive node)
22	BUZZER	PWM signal buzzer control
23	XPWRON	Power key (active low)
24	VA1	Analog supply voltage 4.65 V
25	SIMCLK	Clock for SIM data
26	SIMRESET	Reset for SIM
27	VSIM	SIM voltage supply voltage
28	SIMDATA	Serial data for SIM
29	AGND	Analog ground

Internal Signals Between RF and ASIC

Symbol:	Description:	Values:
SCLK	Synthesizer clock	
	• load impedance:	*10 kΩ*
	• frequency:	*3.25 MHz*
SDATA	Synthesizer data	
	• load impedance:	*10 kΩ*
	• data rate frequency:	*3.25 MHz*
SENA1	Synthesizer enable	
	• PLL contr. disabled:	*4.5...4.65...4.8 V*
	• PLL activated:	*0...0.2...0.7 V*
	• current:	*50 µA*
RXPWR	RX supply voltage on/off	
	• RX supply voltage on:	*4.5...4.65...4.8 V*
	• RX supply voltage off:	*0...0.2...0.7 V*
	• current:	*0.5 mA*
SYNTHPWR	Supply voltage on/off	
	• RF regulators on:	*4.5...4.65...4.8 V*
	• RF regulators off:	*0...0.2...0.7 V*
	• current:	*1.0 mA*
TXPWR	TX supply voltage on/off	
	• TX supply voltage on:	*4.5...4.65...4.8 V*
	• TX supply voltage off:	*0...0.2...0.7 V*
	• current:	*0.5 mA*
TXP	TX enable	
	• transmitter power enable:	*4.5...4.65...4.8 V*
	• transmitter power disable:	*0...0.2...0.7 V*
CLKIN	26 MHz clock to ASIC	

Internal Signals Between RF and RFI

Symbol:	Description:	Values:
AFC	Automatic frequency control voltage	
	• voltage min/max:	*0.35...4.35 V*
	• resolution:	*11 bits*
	• load impedance (dynamic):	*10 kΩ*
TXC	TX transmit power control voltage	
	• voltage range min/max:	*0.3...4.2 V*
	• impedance:	*10 kΩ*
TXQP,TXQN	Differential TX quadrature signal	
	• differential voltage swing:	*1.15...1.2...1.25 V_{PP}*
	• D.C. level:	*2.30...2.35...2.40 V*
	• load impedance:	*30 kΩ*
TXIP,TXIN	Differential TX inphase signal	
	• differential voltage swing:	*1.15...1.2...1.25 V_{PP}*
	• D.C. level:	*2.30...2.35...2.40 V*
	• load impedance:	*30 kΩ*
PDATA0	Front end AGC control	
	• reduced front end gain:	*0...0.2...0.7 V*
	• normal front end gain:	*4.5...4.65...4.8 V*
	• current:	*0.1 mA*
RXQ	RX quadrature signal	
	• output level:	*25 mV_{PP}*
	• source impedance:	*470 Ω*
RXI	RX inphase signal	
	• output level:	*25 mV_{PP}*
	• source impedance:	470 Ω

Functional Description of Baseband Block

The purpose of the baseband module is to control the phone and process audio signals to and from RF. The module also controls the user interface.

Technical Specifications

There are three different operation modes:

– active mode

– idle mode

– power off mode

In the active state all circuits are powered and part of the module may be in idle mode.

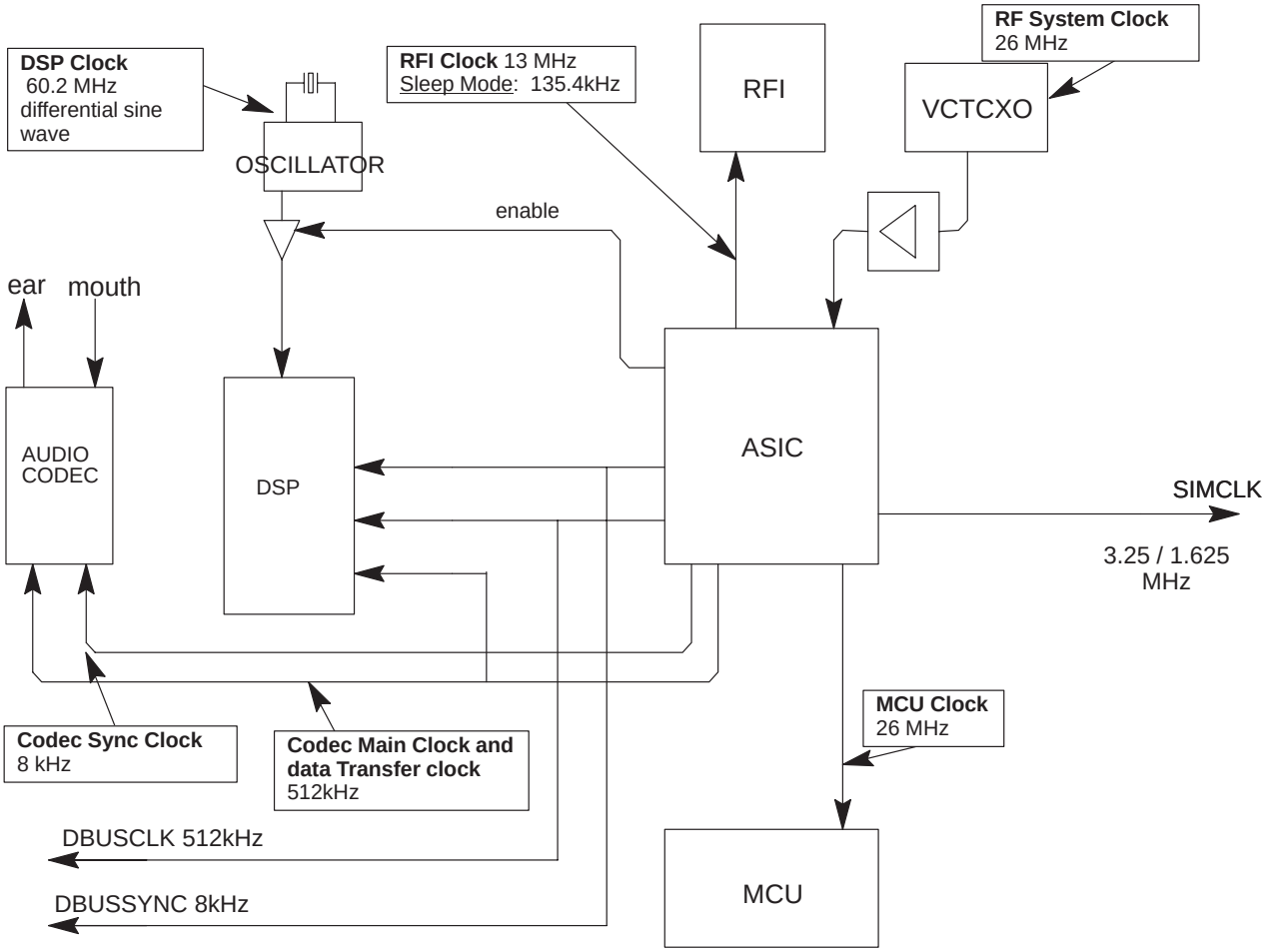
The module is usually in the idle mode when there is no call and the phone is in SERV. In the idle mode circuits are reset, powered down and clocks are stopped or the frequency reduced. All the clocks except the main clock from VCTCXO can be stopped in that mode. Whether the SIM clock is stopped or not depends on the network.

In power off mode only the circuits needed for power up are powered. This means that only power up block inside the PSL+ is powered. The power key on the flex is pulled up with a pull up resistor inside the PSL+.

Names of Functional Blocks

Name:	Function:
CTRLU	Control unit for phone
PWRU	Power supply
DSPU	Digital signal processing block
AUDIO	Audio coding
ASIC	D2CA GSM/PCN system ASIC; several functions
RFI	RF baseband interface

Clocking Scheme



Most of the clocks are generated from the 26 MHz VCTCXO frequency by the ASIC:

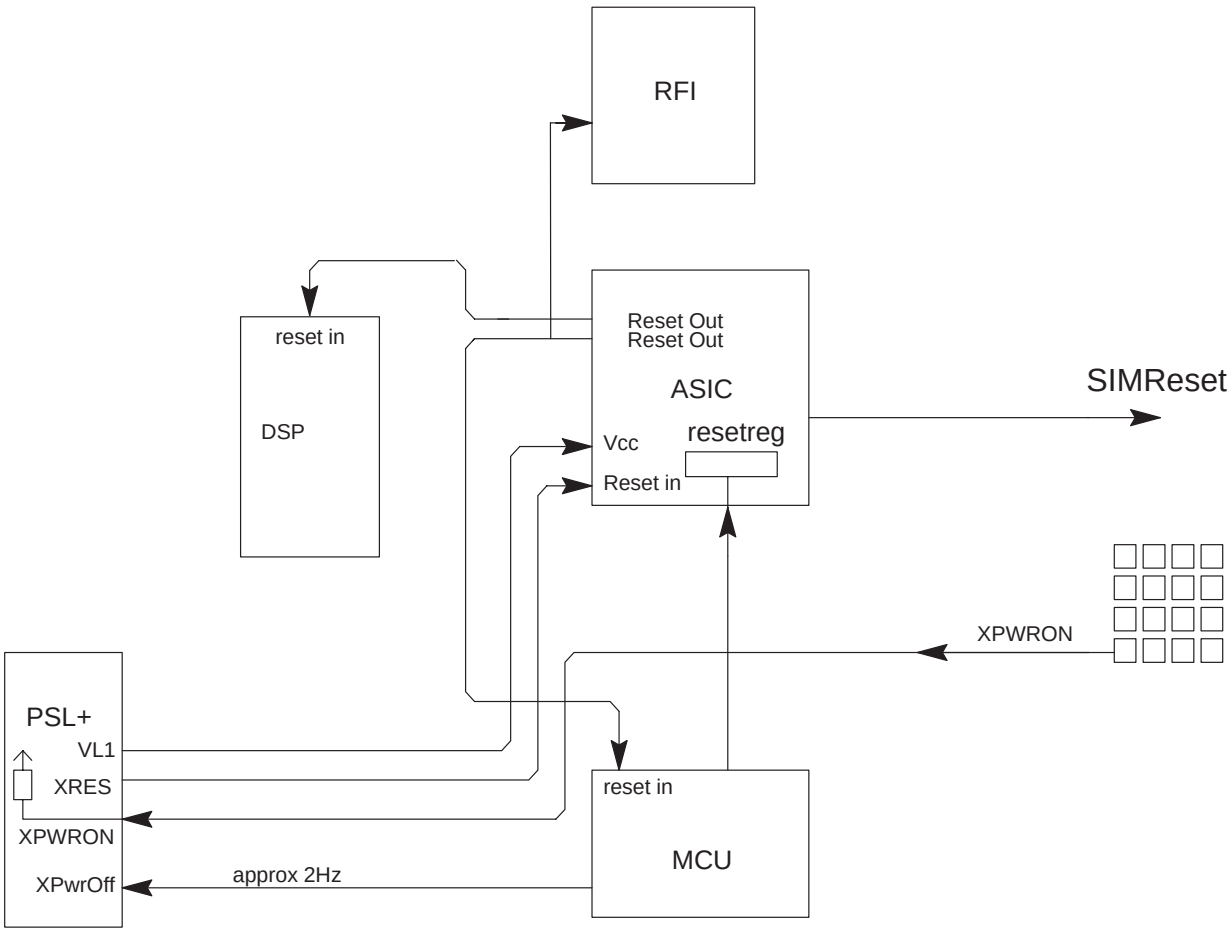
- 26 MHz clock for the MCU. MCU‘s internal clock frequency is half of that (13 MHz).
- 13 MHz for the RFI. The ASIC also generates 135.4 kHz sleep mode clock for the RFI.
- 3.25 MHz clock for SIM. When there is no data transfer between the SIM card and the HP the clock can be reduced to 1.625 MHz. Some SIM cards also allows the clock to be stopped in that mode.
- 512 kHz main clock for the codec and for the data transfer between the DSP and the codec.
- 8 kHz synchronization clock for data transfer between the DSP and the co-dec.
- 512 kHz clock and 8 kHz sync. clock for the DBUS data transfer.

The DSP has its own crystal oscillator which can be turned off and on by the ASIC. The DSP uses differential sinusoidal clock. The frequency is 60.2 MHz.

The system ASIC generates 8 kHz clock to the codec for the control data transfer.

In the idle mode all the clocks can be stopped except 26 MHz main clock coming from the VCTCXO.

Reset and Power Control



There are three different ways to switch power on:

– Power key pressing grounds the XPWRON line. The PSL+ detects that and switches the power on.

– Charger detection on PSL+ detects that charger is connected and switches power on.

– PSL+ will switch power on when the battery is connected. After that the MCU will detect if power key is pressed or charger connected. If not the power will be switched off.

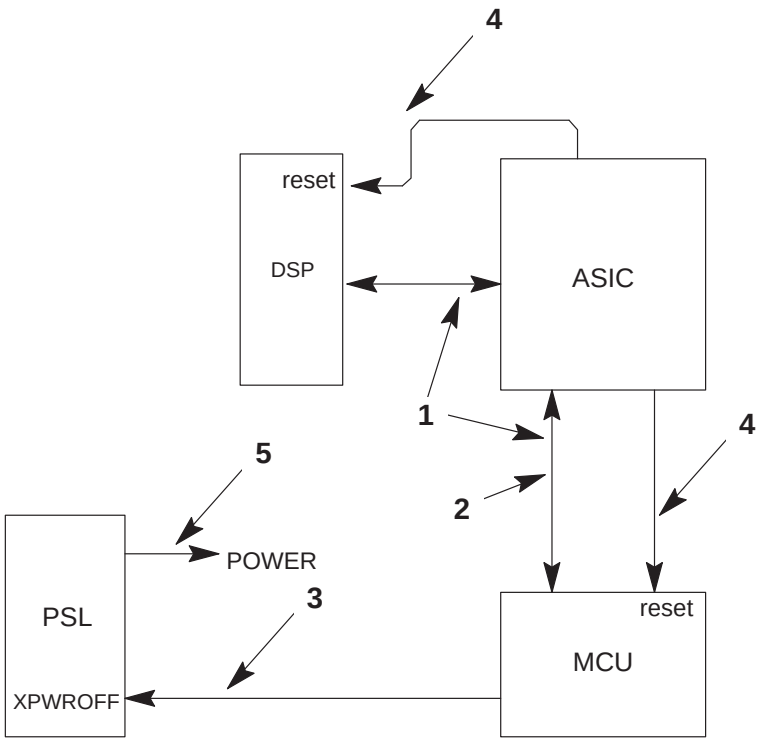
All devices are powered up at the same time by the PSL+. It supplies the reset to the ASIC at power up. The ASIC starts the clocks to the DSP and the MCU. After 100 ms PSL+ releases the reset to ASIC.

ASIC releases MCU and RFI reset after 256 13 MHz clock cycles. DSP reset release time from DSP clock activation can be selected from 0 to 255 13MHz clock cycles. In our case it is 255. SIM reset release time is according to GSM SIM specifications.

To turn power off the user presses the PWR key. The MCU detects this. The MCU cuts off any ongoing call, exits all tasks, acts inoperative to the user and leaves the PSL+ watchdog without resets. After power–down delay, the PSL+ cuts off the supply from all circuitry.

If charging is on the phone stays on but it looks to the user like it is powered off (lights are off and the display is blank) except the charging indicator stays on.

Watchdog System



Normal operation:

1. MCU tests DSP
2. MCU updates ASIC watchdog timer (> 2 Hz)
3. MCU pulses the XPWROFF input on the PSL+ (about 2 Hz)

Failed operation:

4. ASIC resets MCU and DSP after about 0.5 s failure
5. PSL+ switches power off about 1.5 s after the previous XPWROFF pulse

CTRLU

The Control block contains a microcontroller unit (MCU) and three memory circuits (FLASH, SRAM, EEPROM), a 20 bit address bus, an 8 bit data bus and memory circuit control signals.

Main Features of the CTRLU block:

MCU functions:

- system control
- communication control
- user interface
- authentication
- RF monitoring
- power up/down control
- accessory monitoring
- battery monitoring and charging control
- self–test and production testing
- flash loading

Main Components of CTRLU

- Hitachi H8/536

  H8/536 is a CMOS microcontroller unit (MCU) comprising a CPU core and on–chip supporting modules with 16–bit architecture. The data bus to outside world has 8 bits.

- 1024k*8bit FLASH memory
  - 150 ns. maximum read access time with 1 wait state
  - contains the main program code for the MCU; part of the DSP program code also located on FLASH
  - ASIC can address two 4 Mbit memories or one 8 Mbit memory.
- 32 k x 8 bit SRAM memory
  - 100 ns. maximum read access time
- 8 k x 8 bit EEPROM memory
  - 250 ns. maximum read access time with 1 wait state
  - contains user defined information.
  - there is a register bit on the ASIC which must be set before the write operation to the EEPROM.

Input Signals of CTRLU

Name(from):	Description:
VL1(PWRU)	Power supply voltage for CTRLU block
VREF(PWRU)	Reference voltage for MCU A/D converter
VBATDET(PWRU)	Battery voltage detection
VC(PWRU)	Charger voltage monitoring
ROMAD18(ASIC)	ROM address (paging)
EROMSELX(ASIC)	Chip select for the EEPROM memory
ROMSELX(ASIC)	Chip select for the FLASH memory
ROM2SELX(ASIC)	Chip select for the second FLASH memory
RAMSELX(ASIC)	Chip select for the SRAM memory
RESETX(ASIC)	Reset signal for MCU
NMI(ASIC)	Non–maskable interrupt request
MCUCLK(ASIC)	Main clock for MCU
IRQX(ASIC)	Interrupt request
PCMCDO(AUDIO)	Audio codec control data receiving
TRF(RF)	RF module temperature detection
VF(syst.conn.)	Programming voltage for FLASH memory
RXD2_HOOK (syst.conn.)	The use of handsfree monitoring FLASH programming data input on the production line
TBAT(batt.conn.)	Battery temperature detection. Vibra cont. for vibrabattery.
BTYPE(batt.conn.)	Battery size identification
MIC_JCONN (sys.conn.)	Junction box connection identification

Output Signals of CTRLU

Name(to):	Description:
XPWROFF(PWRU)	Power off control, PSL+ watchdog reset
PWM(PWRU)	Charger on/off control
VOLTLIM(PWRU)	Voltage limiting; affects to HW voltage limit level
WSTROBEX(ASIC)	MCU write strobe
RSTROBEX(ASIC)	MCU read strobe
MCUAD(19:0)(ASIC)	20 bit MCU address bus
MBUSDET(ASIC)	MBUS activity detection

BATDET(ASIC)	Battery type and SIM card presence detection
PCMCLK(AUDIO)	Clock for audio codec control data transfer
PCMCDI(AUDIO)	Audio codec control data transmitting
XSELPCMC(AUDIO)	Chip select for audio codec
TXD2_PHFS (syst.connector)	Power on/off control for HF device, verification output of the programmed data of FLASH during programming
CALL_LED(UIF)	'Incoming' call indicator light control
BACKLIGHT(UIF)	LCD and display backlight on/off control
BUZZER(UIF)	Buzzer signal

Bidirectional Signals of CTRLU

Name(to/from):	Description:
MCUDA(7;0)(ASIC)	MCU's 8 bit data bus
M2BUS(sys. conn)	Asynchronous serial data bus

Block Description of CTRLU

– MCU – memories

The MCU has a 20 bits wide address bus A(19:0) and an 8 bit data bus with memories. The address bits A(19:16) are used for chip select decoding. The decoding is done in the D2CA ASIC. The ASIC can address two 4 Mbit (or smaller) or one 8 Mbit flash memories. Hitachi HD647536 processor has internal ROM and RAM memories. One wait state is used with external memory access.

On the Hitachi HD647536 internal memory map there is the following:

- 00000 – 001FF Vector tables
- 00200 – 0F67F 62 k bytes internal ROM
- 0F680 – 0FE7F 2 k bytes internal RAM
- 0FE80 – 0FFFF 384 bytes register field
- 10000 – 1FFFF 32 k * 8 bytes RAM
- 20000 – 2FFFF 8 k * 8 bytes EEPROM
- 30000 – 3FFFF 26 * 8 bytes ASIC
- 40000 – 7FFFF 2 Mbit Flash, paged by ASIC page bit to 4 Mbit
- 80000 – FFFFF 4 Mbit Flash

Chip select generation:

Chip select:	Page:	A19:	A18:	A17:	A16:
RAM	X	0	0	0	1
EEPROM	X	0	0	1	0
ASIC	X	0	0	1	1
FLASH1 (8 Mbit)	X	1	X	X	X

– Flash programming

In flash programming a special flash programming box and a PC is needed. Loading is done through the bottom connector of HP; multiplexed with HOOK and PHFS line. First MCU goes to minimum mode (MBUS command from PC or if MBUS is connected to MIC_JCONN line in power up). Then the flash software is loaded from PC to flash loading box. When the loading is complete flash loading to HP can be started by MBUS command from PC to the MCU. After that the MCU asks the test box to start flash loading to HP. The box supplies 12 V programming voltage for flash and starts to send 250 bytes data blocks to the MCU via HOOK line. The baud rate is 406 kbit/s. The MCU calculates the check sum, sends acknowledge via PHFS line and sends the data to flash. When all the data is loaded the HP makes reset and tells the flash loading box if the loading was succeeded or not. Only PSL+, ASIC and MCU must be active during the loading.

– CTRLU – PWRU

MCU controls the watchdog timer in PSL+. It sends a positive pulse at approximately 2 Hz to XPWROFF pin of the PSL+ to keep the power on. If MCU fails to deliver this pulse, the PSL+ will remove power from the system. MCU also controls the charger on/off switching in the PWRU block. When power off is requested or MCU leaves PSL+ watchdog without reset. After the watchdog time has elapsed PSL+ cuts off the supply voltages from the phone.

– CTRLU – ASIC

MCU and ASIC have a common 8–bit data bus and a 9–bit address bus. Bits A(4:0) are used for normal addressing whereas bits A(19:16) are decoded in ASIC to chip select inputs for CTRLU memories. ASIC controls the main clock, main reset and interrupts to MCU. The internal clock of MCU is half the MCUCLK clock speed. RESETX resets everything in MCU except the contents of the RAM. IRQX is a general purpose interrupt request line from ASIC. After IRQX request the interrupt register of the ASIC is read to find out the reason for interrupt. NMI interrupt is used only to wake up MCU from software standby mode.

– CTRLU – DSPU

MCU and DSP communicate through ASIC. ASIC has an MCU mailbox and a DSP mailbox. MCU writes data to DSP mailbox where DSP can only read the incoming data. In MCU mailbox the data transfer direction is the opposite. When power is switched on the MCU loads data from the flash memory to DSP‘s external memory through this mailbox.

– CTRLU – AUDIO

When the the chip select signal XSELPCMC goes low, MCU writes or reads control data to or from the speech codec registers at the rate defined by PCMCLK. PCMCDI is an output data line from MCU to codec and PCMCDO is an input data line from codec to MCU.

– CTRLU – RF/BATTERY monitoring

MCU has internal 8 channel 10 bit AD converter. Following signals are used to monitor battery, charging and RF:

– BTYPE	battery size
– TBAT	battery temperature (used also for vibrabattery control)
– VBATDET	battery voltage
– VC	charging voltage
– TRF	RF temperature

– CTRLU – keyboard and LCD driver interface

MCU and user interface communication is controlled through ASIC.

– CTRLU – ACCESSORIES

M2BUS is used to control external accessories. This interface can also be used for factory testing and maintenance purposes.

There are also some control and indication signals for the accessories:

– PHFS is used to turn power on to HF accessories.
– JCONN is used to indicate that junction box is connected. Phone can also enter minimum mode when M2BUS is connected to MIC_JCONN line.
– HOOK is used to indicate accessories hook state.
– TBAT is used to control vibrabattery. (Used also for monitoring battery temperature.)

PWRU

The power block creates the supply voltages for the baseband block and contains the charging electronics.

Main Components of PWRU

– PSL+ ASIC

  Generates voltages, contains power on switch, charger and battery voltage detector and watchdog.

– Transistor BCP69–25 and schottky STPS340U

  The charging current is passed through these components.

– Transistor BCX51 and BCP69–25

  VL regulators of PSL+ external output transistors.

Input Signals of PWRU

Name(from):	Description:
XPWRON(UIF)	PWR on switch
XPWROFF(CTRLU)	Power off control
VOLTLIM(CTRLU)	Voltage limiting; affects HW voltage limit level
VBATT(syst.conn.)	Battery voltage
PWM(CTRLU)	Charger on/off control
VCHAR(syst.conn.)	Charging voltage

Output Signals of PWRU

Name(from):	Description:
XRES(ASIC)	Master reset
CHRDET(ASIC)	Battery charger detection
VL1(CTRLU,ASIC, RFI,UIF)	Logic supply voltage, max 150 mA
VL2(DSPU)	Logic supply voltage, max 150 mA
VA1(AUDIO,UIF)	Analog supply voltage, max 40 mA
VA2(RFI)	Analog supply voltage, max 80 mA
VREF(CTRLU,RF)	Reference voltage 4.65 V ±2 %, max 5 mA
VBATDET(CTRLU)	Switched VBATT divided by 2
VC(CTRLU)	Attenuated VCHAR

Block Description of PWRU

The PSL+ IC produces the following supply voltages:

Name:	Description:
VL1, VL2	150 mA for logic
VA1	40 mA for audios
VA2	80 mA for RFI
VREF	5 mA reference

In addition, it has internal watchdog, voltage detection and charger detection functions. The watchdog will cut off output voltages if it is not reset once in every 1.5 (±0.75) second. The voltage detector resets the phone if the battery voltage falls below 4.8 V (±0.2 V). The charger detection starts the phone if it is in power–off state when the charging voltage is applied.

The charging electronics is controlled by the MCU. When the charging voltage is applied to the phone and the phone is powered up, the MCU detects it and starts controlling charging. If MCU detects too high charging voltage (over 14 volts) or current (over 78 A/D bit difference between VC and VBATDET) it will cut off the charging. The phone will accept charging voltages from 5 to 14 volts.

If the phone is in power–off state, the PSL+ will detect the charging voltage and turn on the phone. If the battery voltage is high enough the reset will be released and the MCU will start controlling charging. If the battery voltage is too low the phone stays in reset state and the charging control circuitry will pass charging current to the battery. When the battery voltage has reached 5.25 V (± 0.2 V) the reset will be removed and the MCU starts controlling charging.

MCU controls the charging with pulse width modulation output. Charging voltage is limited by hardware in normal operation to 8.9 V and during a call to 7.6 V.

Battery and charging voltages are calibrated in production; 6V is fed to the battery and charger pin and the MCU‘s A/D converter values are stored to EEPROM.

DSPU

Main interfaces of the DSP:

- MCU via ASIC mailbox
- ASIC
- audio codec
- data bus interface (DBUS) for accessories
- digital audio interface (DAI) for type approval measurements

Main features of the DSP block:

- speech processing
    - speech coding/decoding
        - RPE–LTP–LPC (regular pulse excitation long term prediction linear predictive coding)
    - voice activity detection (VAD) for discontinuous transmission (DTX)
    - comfort noise generation during silence
    - acoustic echo cancellation
- channel coding and transmission
    - block coding (with ASIC)
    - convolutional coding
    - interleaving
    - ciphering (with ASIC)
    - burst building and writing it to ASIC
- Reception
    - reading the A/D conversion results from ASIC
    - impulse response calculation
    - matched filtering
    - bit detection (with Viterbi on ASIC)
    - deinterleaving of soft decisions
    - convolutional decoding (with Viterbi)
    - block decoding (with ASIC)
- Adjacent cell monitoring
    - signal strength measurements
    - neighbor timing measurements
    - neighbor parameter reception

- control functions
  - RF controls
    - synthesizer control
    - power ramp programming
    - automatic gain control (AGC)
    - automatic frequency control (AFC)
  - frame structure control
    - control the operations during a TDMA frame (with ASIC)
    - controlling the multiframe structure
    - channel configuration control
- test functions
  - functions for RF measurements
  - debugging functions for product development

Main Components of DSPU

- AT&T DSP 1616–S11
  - Digital signal processor with 12 kword internal ROM
- Two 32 k * 8 70 ns SRAMs for DSP external memory
- 60.2 MHz crystal osc. to generate differential small signal clock for the DSP

Input Signals of DSPU

Name(from):	Description:
VL2(PWRU)	Logic supply voltage, max 150 mA
DSPCLKEN(ASIC)	Clock enable for DSP clock oscillator circuit
DSP1RSTX(ASIC)	Reset for the DSP
PCMDATRCLKX (ASIC)	PCM data input clock DBUS data output clock
CODEC_CLK	PCM data output clock
PCMOUT(AUDIO)	Received audio in PCM format
DBUSCLK	DBUS data output clock
DBUSSYNC	DBUS data bit sync clock
RDA	DBUS received data
INT0, INT1(ASIC)	Interrupts for the DSP
PCMCOSYCLKX (ASIC)	PCM data bit sync clock

Output Signals of DSPU

Name(to):	Description:
PCMIN(AUDIO)	Transmitted audio in PCM format
IOX(ASIC)	I/O enable, indicates access to DSP address space
RWX(ASIC)	Read/write X
DSPAD(16;9)(ASIC)	Address bus and control signals
DBUSDET(ASIC)	DBUS activity detection

Bidirectional Signals of DSPU

Name(from/to):	Description:
DSPDA(15;0)(ASIC)	16 bit data bus

Block Description of DSPU

The Control unit communicates with the DSP circuitry through a mailbox in the D2CA ASIC. The software for the external memories are loaded through this mailbox in start up.

The DSP includes two serial busses. One is used for speech data transfer between the DSP and the codec. The other is used as an external data bus and it is connected to the bottom connector. This bus can be used by data accessories and also as a digital audio interface (DAI) in audio type approval measurements. The clocks (512 kHz main clock and 8 kHz sync. clock) are generated by the ASIC.

In transmit mode the DSP codes the speech and routes the resulting transmit slots to the D2CA. The D2CA ASIC controls timing, and at specified intervals sends these bits to the RFI for DA conversion.

In digital receive mode the RFI AD converts the IF signal from the RF unit under the control of the D2CA. The DSP controls the D2CA and receives the converted bits. After channel and speech decoding, bits are converted into an analog signal in the PCM codec, routed and fed to the earpiece.

The DSP controls the RF through the D2CA ASIC, where all necessary timing functions are implemented, and control I/O lines are provided e.g. for synte loading.

The DSP emulator can be connected to DSP pins TCK, TMS, TDO, TDI, GND and VDD.

AUDIO

The AUDIO block consists of an audio codec with some peripheral components. The codec contains microphone and earpiece amplifier and all the necessary switches for routing. The codec is controlled by the MCU. The PCM data comes from and goes to the DSP.

Main Components of AUDIO

– Audio codec ST5080

Includes e.g. PCM codec, audio routing switches, microphone and earpiece amplifiers for 2 connections (internal and external devices) and DTMF generator.

Input Signals of AUDIO

Name(from):	Description:
VA1(PWRU)	Analog supply voltage, max 40 mA
PCMIN(DSPU)	Received audio in PCM format
SYNC(ASIC)	8 kHz frame sync
CODEC_CLK(ASIC)	512 kHz codec main clock
PCMCDI(CTRLU)	Audio codec control data
PCMCLK(CTRLU)	Clock for audio codec control data transfer
XSELPCMC (CTRLU)	Audio codec chip select
MIC_JCONN (syst.conn.)	External microphone
MICN,MICP(UIF)	Differential microphone signal

Output Signals of AUDIO

Name(to):	Description:
PCMOUT(DSPU)	Transmitted audio in PCM format
PCMCDO(CTRLU)	Audio codec control data
MIC_ENA(UIF)	Microphone enable
EAR_HFPWR (syst.conn.)	External received audio
EARN,EARP(UIF)	Internal received audio
JCONN(CTRLU)	Junction box connected signal (multiplexed with HFMIC)

Block Description of AUDIO

The codec has two microphone inputs and two earphone outputs. Handportable and external audios can therefore be connected directly to the codec. The codec has internal switches to select which input or output is used. It also has microphone amplifier and earphone attenuator. Input/output selection and amplification/attenuation can be done with codec register settings. The register control is done by the MCU.

Handportable microphone and earphone (located on the flex) are connected directly to the codec‘s differential input and output. External audios are connected single sided. There is 21 dB attenuation in the external microphone line before the codec to prevent clipping.

Microphone signal is routed to the microphone amplifier. After that it is fed to the bandpass filter and then to the A/D converter. After the conversion the digital speech is sent to the DSP.

Digital downlink signal from the DSP is fed to the D/A converted. After the converter there is low pass filter and attenuator before the earphone output. All these are inside the codec. The ASIC generates the 512 kHz and 8 kHz clocks for the codec and data transmission between the codec and the DSP

The audio codec communicates with the DSP (analog speech) through an SIO (signals: PCMIN, SYNC, CODEC_CLK and PCMOUT) . The MCU controls the audio codec function through a separate serial bus (signals: PCMCDO, PCMCDI, PCMCLK and XSELPCMC).

The codec generates DTMF tones (key beeps) to the earphone and in HF mode to the external speaker. In portable mode the MCU generates ringing tones and also some warning tones to the buzzer. In HF mode they are generated by the codec and driven to the external speaker line. Several tones are network originated. Depending on network transceiver is either commanded to generate tone, or network sends the tone itself.

One codec output pin is used to switch on/off the microphone bias circuit on the flex.

External microphone line is used also to detect if junction box is connected to the bottom connector. Microphone signal is therefore routed to the MCU A/D converter.

Also external earphone signal is multiplexed. 100 kΩ pull down resistor is used to turn power on to the HF accessories.

ASIC

The ASIC takes care of the following functions:

- interface between MCU and UIF
- interface between MCU, DSP and RFI
- hardware accelerator functions to DSP
- clock generation and disable/enable
- RF controls
- UIF interface
- timers
- M2BUS interface
- SIM interface

Main Components of ASIC

- D2CA ASIC
- RFC buffer

  Inverter buffer stage is used as a buffer for the VCTCXO clock.

Input Signals of ASIC

Name(from):	Description:
VL1(PWRU)	Logic supply voltage, max 150 mA
VL2(PWRU)	Logic supply voltage, max 150 mA
CHRDET(PWRU)	Battery charger detection
IOX(DSPU)	I/O enable, indicates access to DSP address space
RWX(DSPU)	Read/write X
WSTROBEX (CTRLU)	MCU’s write strobe
RSTROBEX (CTRLU)	MCU’s read strobe
RFC(RF)	Reference clock from VCTCXO
XRES(PWRU)	Master reset
DSPAD(16;0)(DSPU)	Address bus and control signals
MCUAD(19;16,4;0) (CTRLU)	MCU’s address bus
DAX(RFI)	Data acknowledge
BATDET(CTRLU)	Battery type and SIM card presence detection

MBUSDET(CTRLU)	MBUS activity detection
DBUSDET(DSPU)	DBUS activity detection

Output Signals of ASIC

Name(to):	Description:
INT0,INT1(DSPU)	Interrupts for DSP
NMI(CTRLU)	Not maskable interrupt request
IRQX(CTRLU)	Interrupt request
RESETX (CTRLU,RFI)	Master (power µp) reset
DSP1RSTX(DSPU)	Reset for the DSP
SIMRESET	Reset for the SIM
WRX(RFI)	Write strobe
RDX(RFI)	Read strobe
RFIAD(3;0)(RFI)	RFI address bus
SCLK(RF)	Synthesizer load clock
SDATA(RF)	Synthesizer load data
SENA1(RF)	UHF and VHF PLL enable
RXPWR(RF)	RX circuitry power enable
TXPWR(RF)	TX circuitry power enable
SYNTHPWR(RF)	Synthesizer circuitry power enable
TXP(RF)	Transmitter power control enable
MCUCLK(CTRLU)	Main clock for MCU
DSPCLKEN(DSPU)	DSP clock circuit enable
RFICLK(RFI)	RFI master clock
RFI2CLK(RFI)	RFI sleep clock
CODEC_CLK (DSPU,AUDIO)	PCM data clock
PCMDATRCLKX (DSPU)	Inverted PCM data clock, used as input clock for codec and DBUS interface
SYNC(AUDIO)	Bit sync clock
PCMCOSYCLKX (DSPU)	Bit sync clock, inverted
DCLK(syst.conn.)	DBUS data clock
DSYNC(syst.conn.)	DBUS bit sync clock

DBUSCLK(DSPU)	DBUS data clock
DBUSSYNC(DSPU)	DBUS bit sync clock
SIMCLK(UIF)	SIM data clock
VSIM(UIF)	SIM power control
ROMAD18(CTRLU)	ROM address (paging)
ROMSELX(CTRLU)	Chip select for the FLASH memory
ROM2SELX (CTRLU)	Chip select for the second FLASH memory
EROMSELX (CTRLU)	Chip select for the EEPROM memory
RAMSELX(CTRLU)	Chip select for the SRAM memory
COL(3;0)(UIF)	Lines for keyboard column write

Bidirectional Signals of ASIC

Name(from/to):	Description:
DSPDA(15;0) (DSPU)	16 bit data bus
MCUDA(7;0) (CTRLU)	MCU’s 8 bit data bus
RFIDA(11;0)(RFI)	12 bit data bus
UIF(6;0)(UIF)	LCD controller control and keyboard read bus
SIMDATA(UIF)	Serial data to SIM

Block Description of ASIC

PSL+ supplies the reset to the ASIC at power up. The ASIC starts the clocks to the DSP and the MCU. MCU and RFI reset is released after 256 13 MHz clock cycles. DSP reset release time from DSP clock activation can be selected from 0 to 255 13 MHz clock cycles. In our case 255 is selected. SIM reset release time is according to GSM SIM specifications.

The RFC buffer buffers the 26MHz clock from the VCTCXO to the ASIC. In the ASIC the clock is further buffered and divided for the MCU, RFI, SIM. It also generates main and sync clocks for audio codec, DSP‘s SIOs and DBUS. The clock outputs can be disabled in order to save current when the clock is not needed. Also the DSP oscillator can be stopped by the ASIC.

Interface to the MCU is done with 8 bit data bus ,5 bit lower address bus, 4 bit upper address bus, RSTRBEX, WSTROBEX, IRQX and NMI. ASIC is in the same memory space as MCU memories. The ASIC generates chip selects from the address bits A16–19. There is also M2BUS detector and netfree counter on the ASIC. Netfree interrupt IRQX occurs if no activity is detected in M2BUS in about 3ms. NMI is used to wake up the MCU from sleep mode.

MCU and DSP communicate through ASIC. ASIC has an MCU mailbox and a DSP mailbox. MCU writes data to DSP mailbox where DSP can only read the incoming data. In MCU mailbox the data transfer direction is the opposite. The size of the mailbox is 64 * 8 bit.

MCU and User Interface (keyboard and display) communication is controlled through the ASIC.

COL(0–3) are used as column lines in keyboard. UIF(0–5) are used as row lines They are also multiplexed with display driver control signals.

When a key is pressed the ASIC generates an interrupt from low input of row and starts scanning. One column at the time is written to low and rows are used to read which key it was.

Row lines and UIF6 are used for display driver control. UIF(0–3) are used as 4 bit parallel data bus for the LCD driver. UIF4 is used as read/write strobe, UIF5 to select data or instruction register and UIF6 as enable strobe.

The SIM interface is the electrical interface between the smart card used in the GSM and PCN applications and the MCU via the ASIC. ASIC converts the serial data received from the SIM to parallel data for MCU and converts parallel data from MCU to serial mode for the card. The SIM interface also takes care of the power up and down procedure to the card, frame and parity error checking. The communication between card and ASIC is asynchronous and half duplex. Four signals are used between the ASIC and the SIM card: SIMDATA, SIMCLK, SIMRESET and The clock frequency is 3.25 MHz. When there is no data transfer between the SIM card and the HP the clock can be reduced to 1.625 MHz. Some SIM cards also allows the clock to be stopped in that mode. Supply voltage VSIM can be switched off by the ASIC. The supply voltage is 4.65 V. The carddetect input on the ASIC is connected to BTYPE pin and when the battery is removed the ASIC will drive the SIM down.

The interface to the DSP is done using 6 bit address bus, 16 bit data bus, IOX and RWX lines. Data bus is latched using IOX, address bus is not. The ASIC also generates interrupt INT0 when an edge occurs in DBUS line (if the mask bit is off). INT1 is used as RX interrupt and as MFI modulator interrupt to the DSP.

Viterbi is used to perform GSM/PCN convolutional decoding and bit detection according to viterbi algorithm. It can be controlled and accessed thoroughly by the DSP.

Coder is used to perform block encoding, decoding, and ciphering according to GSM algorithm A5 or A5/2. (D2CA supports both algorithms.)

The ASIC takes care of the interface between the DSP and the RFI: TX modulator, RX filter, TX and RX sample buffers and controlling state machine. The interface to RFI is done using 12 bit data bus, 4 bit address bus, RDX and WRX. There is data acknowledge (DAX) from RFI to ASIC. Also in this block are the serial RF synthesizer interface (SCLK, SDAT) and the digital RF control signals (RXPWR, TXPWR, TXP, SYNTHPWR).

RFI

The block consists of RFI ASIC and its reference voltage generator. This block is an interface between RF and baseband. The RFI block has the following functions:

- IF receiving and A/D conversion
- I/Q separation
- I and Q transmit and D/A conversion
- AFC D/A
- TXC
- AGC (in combination with TXC)

Main Components of RFI

- RFI ASIC
- 4.096 V external voltage reference LM4040 for RFI

Input Signals of RFI

Name(from):	Description:
VL1(PWRU)	Logic supply voltage, max 150 mA
VA2(PWRU)	Analog supply voltage, max 80 mA
RESETX(PWRU)	Master (power up) reset
RFIAD(3;0)(ASIC)	RFI address bus
RDX(ASIC)	Read strobe
WRX(ASIC)	Write strobe
RFICLK(ASIC)	RFI master clock
RFI2CLK(ASIC)	RFI sleep clock
RXQ(RF)	RX quadrature signal
RXI(RF)	RX inphase signal

Output Signals of RFI

Name(to):	Description:
DAX(ASIC)	Data acknowledge
AFC(RF)	Automatic frequency control voltage
TXC(RF)	TX transmit power control voltage, AGC control
TXQP,TXQN(RF)	Differential TX quadrature signal
TXIP,TXIN(RF)	Differential TX inphase signal
PDATA0(RF)	Front end AGC data

Bidirectional Signals of RFI

Name(to):	Description:
RFIDA(11;0)(ASIC)	12 bit data bus

Block Description of RFI

The RFI provides A/D conversion of the in–phase (RXI) and quadrature (RXQ) signals in receive path. It has 12 bit sigma–delta A/D converters and the sample rate is 541.667 kHz.

Analog transmit path includes 8 bit D/A converters to generate the in–phase (TXI) and quadrature (TXQ) signals. RFI has differential outputs for TXI and TXQ. The sample rate is 1.0833 MHz.

There is 11 bit D/A converter for automatic frequency correction. The sample rate is 1.3542 kHz.

Power ramp is done with 10 bit D/A converter. The sample frequency is 1.0833 MHz.

The AGC is voltage controlled in HD841. (In HD740 AGC control was digital.) Front end AGC control is done with PDATA0 output. Main part of AGC is controlled by TXC.

The RFI has 12 bit data bus to the ASIC. The registers in the RFI are accessed using 4 address bits. Control and clock signals are coming from the ASIC.

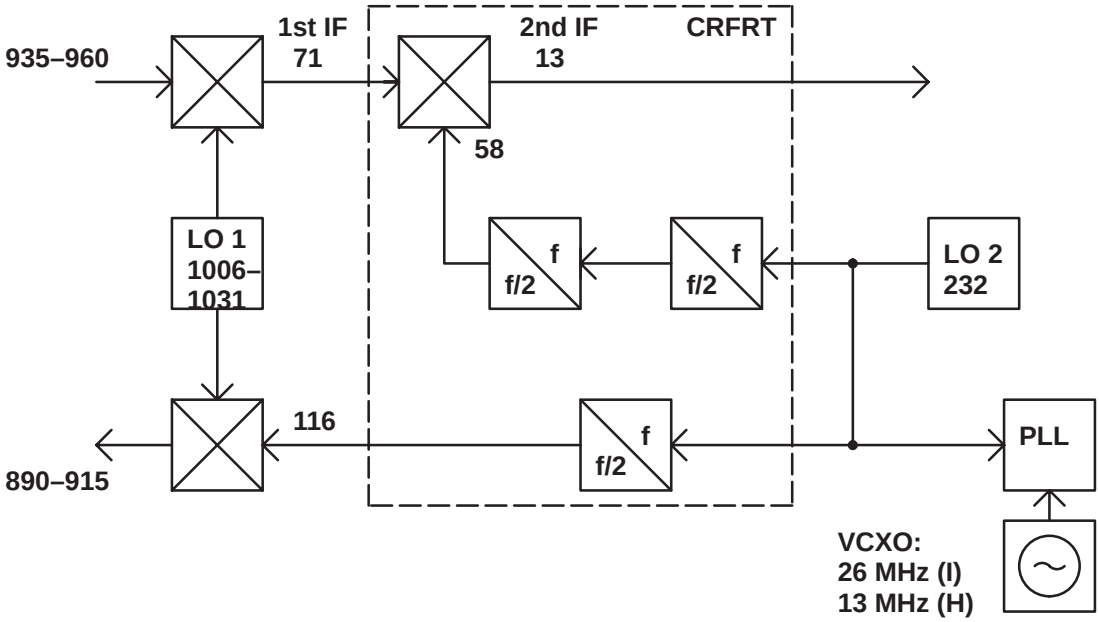
The RFI has external 4.096 V voltage reference.

Functional Description of RF block

The RF block carries out all the RF functions of the transceiver. The RF block works in GSM system.

RF Frequency Plan

GSM



Regulators

There is one regulator IC in the RF unit. The regulator IC CRFCONT is an RF power supply circuit basically intended for digital handportable phones. It has 8 separate linear regulators. Each regulator can be individually disabled and enabled. It also has a voltage reference output.

See more details on Figure; Power Distribution Diagram of RF

Power Distribution

All currents in the power distribution diagram are peak currents. Activity percentages are in SPEECH–mode 24.6 % for RXPWR, 15.8 % for TXPWR and 100 % for SYNTHPWR. In IDLE–mode activities are 0.4 %, 0.0 % and 1.77 % respectively. The current of each block is controlled independently and for example TXPWR and RXPWR are not on at the same time.

Current Consumption

In the following table the RF current consumption can be seen with different status of the control signals. The VCTCXO is not included in the results.

SYNTHPWR:	RXPWR:	TXPWR:	TXP:	Typ. load current:	Notes:
L	L	L	L	0.05 mA	Leakage current
H	L	L	L	41.5 mA	Synthesizer active
H	H	L	L	115.5 mA	Reception
H	L	H	L	93.5 mA	TX active
H	L	H	H	1393.5 mA	Transmission

Receiver

The receiver is a double conversion receiver.

The received RF signal from the antenna is fed via a duplex filter to the receiver unit. The signal is amplified by a discrete low noise preamplifier. The gain of the amplifier is controlled by the AGC control line (PDATA0). The nominal gain of 16.5 dB in GSM is reduced in the strong field condition about 36 dB. After the preamplifier the signal is filtered by SAW RF filter. The filter rejects spurious signals coming from the antenna and spurious emissions coming from the receiver unit.

In GSM the filtered RF signal is down converted by a passive diode mixer. The frequency of the first IF is 71 MHz. The first local signal is generated by the UHF synthesizer.

The IF signal 71 is amplified and filtered by SAW filter in GSM. The filter rejects adjacent channel signal, intermodulating signals and the last IF image signal. The filtered IF signal is fed to the receiver part of the integrated RF circuit CRFRT.

In CRFRT the filtered IF signal is amplified by an AGC amplifier which has gain control range of 57 dB. The gain is controlled by an analog signal via TXC line. The amplified IF signal is down converted to the last IF in the mixer of CRFRT. The last local signal is generated from VHF VCO by dividing the original signal by 4 in the dividers of CRFRT.

The last IF 13 MHz is filtered by a ceramic filter. The filter rejects signals of the adjacent channels.

The filtered last IF is fed back to CRFRT where it is amplified and fed out via RXIF line. IF signal is split to +45 and –45 signals and then fed to RFI.

Duplex Filter

The duplex filter consists of two functional parts; RX and TX filters. The TX filter rejects the noise power at the RX frequency band and TX harmonic signals. The RX filter rejects blocking and spurious signals coming from the antenna.

Pre–Amplifier

The bipolar pre–amplifier amplifies the received signal coming from the antenna. In the strong field conditions the gain of the amplifier is reduced 36 dB in GSM, typically.

Parameter	*Value*
Frequency band:	*935–960 Mhz*
Supply voltage (min/typ/max):	*4.27...4.5...4.73 V*
Current consumption (min/typ/max):	*5...6....7 mA*
Insertion gain (min/typ/max):	*15...16.5...17 dB*
Gain flatness:	*±0.5 dB*
Noise figure (typ/max):	*2.0...2.5 dB*
Reverse isolation (min):	*15 dB*
Gain reduction (min/typ/max):	*33...36...39 dB*
IIP3: (min/typ):	*–12...–10 dBm*
Input VSWR; zo=50 Ω (max):	*2.0*
Output VSWR; zo=50 Ω (max):	*2.0*

RX Interstage Filter

The RX interstage filter is a SAW filter in GSM. The filter rejects spurious and blocking signals coming from the antenna. It rejects the local oscillator signal leakage, too.

First Mixer

The first mixer is a single balanced passive diode mixer. The local signal is balanced by a printed circuit transformer. The mixer down converts the received RF signal to IF signal.

Parameter	*Value*
RX frequency range:	*935–960 Mhz*
LO frequency range:	*1006–1031 Mhz*
IF frequency:	*71 Mhz*
Conversion loss (min/typ/max):	*5...6...7 dB*
IIP3 (min/typ):	*2...5 dBm*
LO – RF isolation (min):	*15.0 dB*
LO power level (min):	*3 dBm*

First IF Amplifier

The first IF amplifier is a bipolar transistor amplifier.

Parameter	*Value*
Operation frequency:	*71 Mhz*
Supply voltage (min/typ/max):	*4.27...4.5...4.73*
Current consumption (typ/max):	*12...20 mA*
Insertion gain (min/typ/max):	*18...20...22 dB*
Noise figure (typ/max):	*3.5...4.0 dB*
IIP3 (min/typ):	*–5...–3 dBm*

First IF filter

The first IF filter is a SAW filter in GSM. The IF filter rejects some spurious and blocking signal coming from the front end of the receiver.

Receiver IF circuit, RX part of CRFRT

The receiver part of CRFRT consists of an AGC amplifier of 57 dB gain, a mixer and a buffer amplifier for the last IF. The mixer of the circuit down converts the received signal to the last IF frequency. After external filtering the signal is amplified and fed to baseband circuitry. The supply current can be switched OFF by an internal switch, when the RX is OFF.

Parameter	*Value*
Supply voltage (min/typ/max):	*4.27...4.5...4.73 V*
Current consumption (max/max):	*35...44 mA*
Input frequency range (min/max):	*45 MHz (–1 db point) ...87 MHz (–3 dB point)*
Local frequency range of mixer (min/max):	*170...400 MHz*
2nd IF range (min/max):	*2...17 MHz*
Voltage gain (max gain) of AGC amplifier (min):	*47 dB*
Noise figure (max):	*15 max gain*
AGC gain control slope (min/typ/max):	*40...84...100 dB/V*
Mixer output 1 dB compression point (typ):	*1.0 V_{PP}*
Max output level after last IF buffer (typ):	*1.6 V_{PP}*

Last IF Filter

The last IF is a ceramic filter, which makes the part of the channel selectivity of the receiver.

Transmitter

The TX intermediate frequency is modulated by an I/Q modulator contained on transmitter section of CRFRT IC. The TX I and Q signals are generated in the RFI interface circuit and they are fed differentially to the modulator.

Modulated intermediate signal is amplified or attenuated in temperature compensated controlled gain amplifier (TCGA). The output of the TCGA is amplified and the output level is typically –10 dBm.

The output signal from CRFRT is band–pass filtered to reduce harmonics and the final TX signal is achieved by mixing the UHF VCO signal and the modulated TX intermediate signal with passive mixer. After mixing the TX signal is amplified and filtered by two amplifier and one filter. This filter is dielectric filter. After these stages the level of the signal is typically 1 mW (0 dBm).

The discrete power amplifier amplifies the TX signal to the desired power level. The maximum output level is typically 1.8...2.0 W.

The power control loop controls the output level of the power amplifier. The power detector consists of a directional coupler and a diode rectifier. Transmitted power is controlled with controlled gain amplifier (TCGA) on TX path of CRFRT. Power is controlled with TXC and TXP signals. The power control signal (TXC), which has a raised cosine form, comes from the RF interface circuit, RFI.

Modulator Circuit, TX part of CRFRT

The modulator is a quadrature modulator contained in TX section of CRFRT IC. The I– and Q– inputs generated by RFI interface are D.C. coupled and fed via buffers to the modulator. The local signal is divided by two to get accurate 90 degrees phase shifted signals to the I/Q mixers. After mixing the signals are combined and amplified with temperature compensated controlled gain amplifier (TCGA). Gain is controlled with power control signal (TXC). The output of the TCGA is amplified and the maximum output level is –10 dBm, typically.

Parameter	*Value*
Supply voltage (min/typ/max):	*4.27...4.5...4.73 V*
Supply current (typ/max):	*36...45 mA*

Transmit frequency input	*Value*
LO input frequency (min/max):	*170...400 MHz*
LO input power level (typ):	*0.2 V_{PP}*
LO input resistance (min/typ/max):	*70...100...130 Ω*
LO input capacitance (typ):	*4 pF*

Modulator Inputs (I/Q):	*Value*
Input bias current, balanced (max):	*100 nA*
Input common mode voltage (min/typ/max):	*2.0...2.2...2.4 V*
Input level, balanced (max):	*1.1 V_{PP}*
Input frequency range (min/max):	*0...300 kHz*
Input resistance, balanced (min):	*200 kΩ*
Input capacitance, balanced (max):	*4 pF*

Modulator Output:	*Value*
Output frequency (min/max):	*85...200 MHz*
Available linear RF power (typ):	*–10 dBm, ZiL=50 kΩ*
Available saturated RF power (min/typ):	*–5...0 dBm, ZiL=50 kΩ*
Total gain control range (min):	*45 dB*
Gain control slope (typ):	*84 dB/V*
Suppression of 3rd order prods (min):	*35 dB*
Carrier suppression (typ):	*35 dB*
Single sideband suppression:	
Noise floor P_{OUT}	
• –10 (max):	*–132 dBm/Hz avg.*
• –18 (max):	*–137 dBm/Hz avg.*
• –24 (max):	*–140 dBm/Hz avg.*
• –30 (max):	*–142 dBm/Hz avg.*
• –40 (max):	*–144 dBm/Hz avg.*
Transmitted I/Q phase balance:	*–5...5 deg*
drift in whole temperature range:	*–2...2 deg*
Transmitted I/Q amplitude balance:	*–0.5...0.5 dB*
drift in whole temperature range:	*–0.2...0.2 dB*

Upconversion Mixer

The upconversion mixer is a single balanced passive diode mixer. The local signal is balanced by a printed circuit transformer. The mixer upconverts the modulated IF signal coming from quadrature modulator to RF signal.

Parameter:	*Value*
RX frequency range:	*890...915 MHz*
LO frequency range:	*1006...1031 MHz*
IF frequency (nom):	*116 MHz*
Conversion loss (min/typ/max):	*6.0...7.0...8.0 dB*
IIP3 (min):	*0.0 dBm*
LO – RF isolation (min):	*15 dB*
LO power level (min):	*3.0 dBm*

TX Interstage Filters

The TX filters reject the spurious signals generated in the upconversion mixer. They reject the local, image and IF signal leakage and RX band noise, too.

1st TX buffer

The TX buffer is a bipolar transistor amplifier. It amplifies the TX signal coming from the upconversion mixer.

Parameter:	*Value*
Operating frequency range:	*890...915 MHz*
Supply voltage (min/typ/max):	*4.25...4.5...2.8 V*
Current consumption (typ/max):	*4.5...5.0 mA*
Insertion gain (min/typ/max):	*11...12...13 dB*
Input VSWR, Zo=50 Ω (max):	*2.0*
Output VSWR, Zo=50 Ω (max):	*2.0*

2nd TX buffer

The TX buffer is a bipolar transistor amplifier. It amplifies the TX signal coming from the first interstage filter.

Parameter:	*Value*
Operation frequency range:	*890...915 MHz*
Supply voltage (min/typ/max):	*4.25...4.5...4.8 V*
Current consumption (typ/max):	*9.0...10.0 mA*
Insertion gain (min/typ/max):	*11...12...13 dB*
Output power, Zo=50 Ω (min/typ):	*0...3 dBm*
Input VSWR, Zo=50 Ω (max):	*2.0*
Output VSWR, Zo=50 Ω (max):	*2.0*

Power Amplifier

The power amplifier is a three stage discrete amplifier. It amplifies the 0 dBm TX signal to the desired output level. It has been specified for 6 volts operation.

Parameter:	*Value*
D.C. supply voltage, no RF (max):	*10 V*
D.C. supply voltage (min/typ/max):	*5.3...6.0...8.5 V*
Operation frequency:	*890...915 MHz*
Operating case temp. range (max):	*90 °C*
Max output power (min/typ/max):	*34.5...35...36 dBm, norm cond.*
Max output power (min/typ/max):	*33.5...34...35 dBm, extreme cond.* V_{CC}*=5.4 V, Ta=55°C*
Input power (min):	*0 dBm*
Gain (min/typ/max):	*34.5...35...36 dB*
Efficiency (typ):	*42 %, Po=35 dBm*
Input VSWR, Zo=50 Ω (max):	*2.0*
Output VSWR, Zo=50 Ω (max):	*2.0*
Harmonics, 2 fo: 3 fo, 4 fo, 5 fo:	*–30 dBc, Po=35 dBm* *–40 dBc, Po=35 dBm*
Noise power (max):	*–114 dBm at receiver band*
Ruggedness (min):	*8 V VSWR=7,* P_{OUT}*=4 W*
Stability, load VSWR 6:1 (min):	*60 dBc, all spurious*

Power Control Circuitry

The power control loop consists of a power detector and a differential control circuit. The power detector is a combination of a directional coupler and a diode rectifier. The differential control circuit compares the detected voltage and the control voltage (TXC) and controls voltage controlled amplifier (in CRFRT) or the power amplifier. The control circuit is a part of CRFRT.

Parameter:	*Value*
Supply voltage (min/typ/max): using CRFRT:	*4.5...4.7...4.9* *4.27...4.5...4.73*
Supply current (typ/max):	*3.0...5.0 mA*
Power control range (min):	*20 dB*
Power control inaccuracy (max):	*±1.0 dB*
Dynamic range (min):	*80 dB*
Input control voltage range (min/max):	*0.1...2.8 V*

Synthesizer

The stable frequency source for the synthesizers and base band circuits is discrete voltage controlled crystal oscillator, VCXO. The frequency of the oscillators is controlled by an AFC voltage, which is generated by the base band circuits.

The UHF PLL generates the down conversion signal for the receiver and the up conversion signal for the transmitter. The UHF VCO is a discrete oscillator. The PLL circuits is UMA1018.

The VHF PLL signal (divided by 4 in CRFRT) is used as a local for the last mixer. Also the VHF PLL signal (divided by 2 in CRFRT) is used in the I/Q modulator of the transmitter chain.

Reference Oscillator

The reference oscillator is a discrete VCXO and the frequency is 26 MHz.

The oscillator signal is used for a reference frequency of the synthesizers and the clock frequency for the base band circuits.

Parameter:	*Value*
Centre frequency:	*26 MHz*
Frequency control range:	*67 ppm*
Supply voltage (min/typ/max):	*4.6...4.7...4.8 V*
Current consumption (typ/max):	*1.5..1.7 mA*
Output voltage (min/typ/max):	*1.3...1.7...2.0 V_{PP}, sine wave for PLLs*
Harmonics (max):	*5 dBc*
Control voltage range (min/max):	*0.25...4.45 V*
Nominal voltage for centre frequency:	*2.2 V*
Control sensitivity (min/typ/max):	*12...16...22 ppm/V*
Frequency stability	
• temperature:	*10 ppm, –25...+75 °C*
• supply voltage:	*1 ppm, 4.7 V ±5 %*
• load:	*0.1 ppm, load ±10 %*
• aging:	*1 ppm, year*
Operating temperature range (min/max):	*–20...70 °C*
Load impedance, resistive part:	*2 kΩ*
parallel capacitance:	*20 pF*

VHF PLL

The VHF PLL consists of the VHF VCO, PLL integrated circuit and loop filter. The output signal is used for the 2nd mixer of the receiver and for the I/Q modulator of the transmitter.

Parameter:	*Value*
Start up setting time (max):	*5 ms*
Phase error (max):	*1 deg., rms*
Sidebands (typ/max)	
• ±200 kHz:	*–75...–70 dB*
• ±400 kHz:	*–84...–70 dB*
• ±1 MHz:	*<–85...–70 dB*
• ±2 MHz:	*<–85...–75 dB*
• ±3 MHz:	*<–85...–80 dB*
• >4 MHz:	*<–85...–80 dB*

VHF VCO + buffer

The VHF VCO uses a bipolar transistor as a active element and a combination of a chip coil and varactor diode as a resonance circuit. The buffer is combined into the VCO circuit so, that they use same collector current.

Parameter:	*Value*
Supply voltage (min/typ/max):	*4.2...4.5...4.8 V*
Control voltage (min/max):	*0.5...4.0 V*
Supply current (typ/max):	*2.5...5.0 mA*
Operation frequency (typ):	*232 MHz*
Output power level (typ):	*168 mV_{RMS}/1 kΩ*
Control voltage sensitivity (typ):	*12 MHz/V*
Phase noise (max)	
• fo ±200 kHz	*–123 dB*
• fo ±1600 kHz	*–133 dB*
• fo ±3000 kHz	*–143 dB*
Harmonics (typ/max):	*–32...–30 dB*

UHF PLL

The UHF PLL consists of a UHF VCO, PLL circuit and a loop filter. The output signal is used for the 1st mixer of the receiver and the upconversion mixer of the transmitter.

Parameter:	*Value*
Start up setting time (max):	*5 ms*
Phase error (max):	*4 deg., rms*
Settling time ±93 MHz (typ/max):	*525...800 µs*
Sidebands (typ/max)	
• ±200 kHz:	*–80...–60 dB*
• ±400 kHz:	*–87...–65 dB*
• ±600 kHz:	*<–90...–70 dB*
• 1.4...3.0 MHz:	*<–90...–80 dB*
• >3.0 MHz:	*<–80 dB*

UHF VCO + buffer

The UHF VCO uses a bipolar transistor as a active element and a combination of a chip coil and a varactor diode as a resonance circuit.

UHF VCO Buffers

The UHF VCO output signal is divided into the 1st mixer of the receiver and the upconversion mixer of the transmitter. The UHF VCO signal is amplified after division. There is one buffer for TX and one for RX.

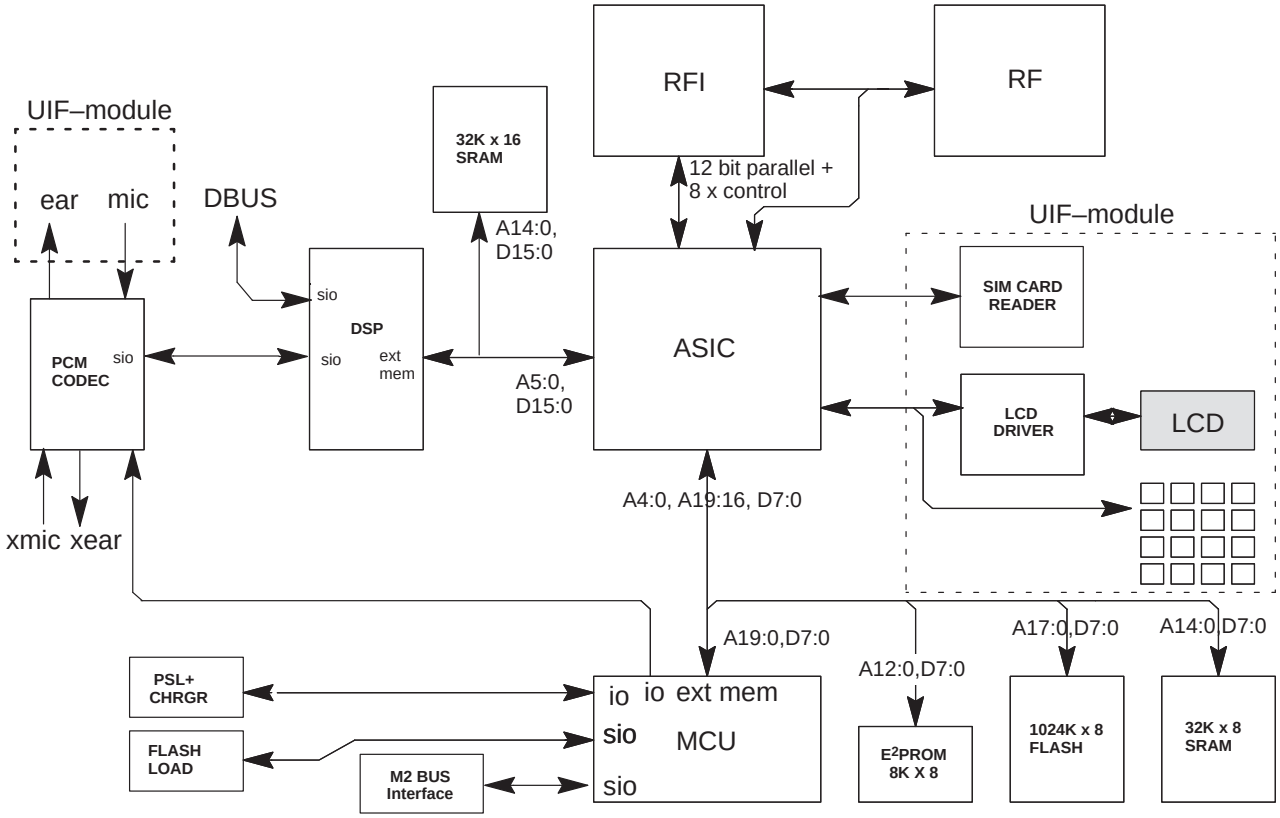
Parameter:	*Value*
Supply voltage (min/typ/max):	*4.2...4.5...4.8 V*
Supply current (typ/max):	*5.5...6.5 mA*
Input power (typ):	*–3 dBm*
Harmonics (max):	*–10 dBc*
Output power (typ):	*700 mV_{RMS}/1 kΩ*

PLL Circuit

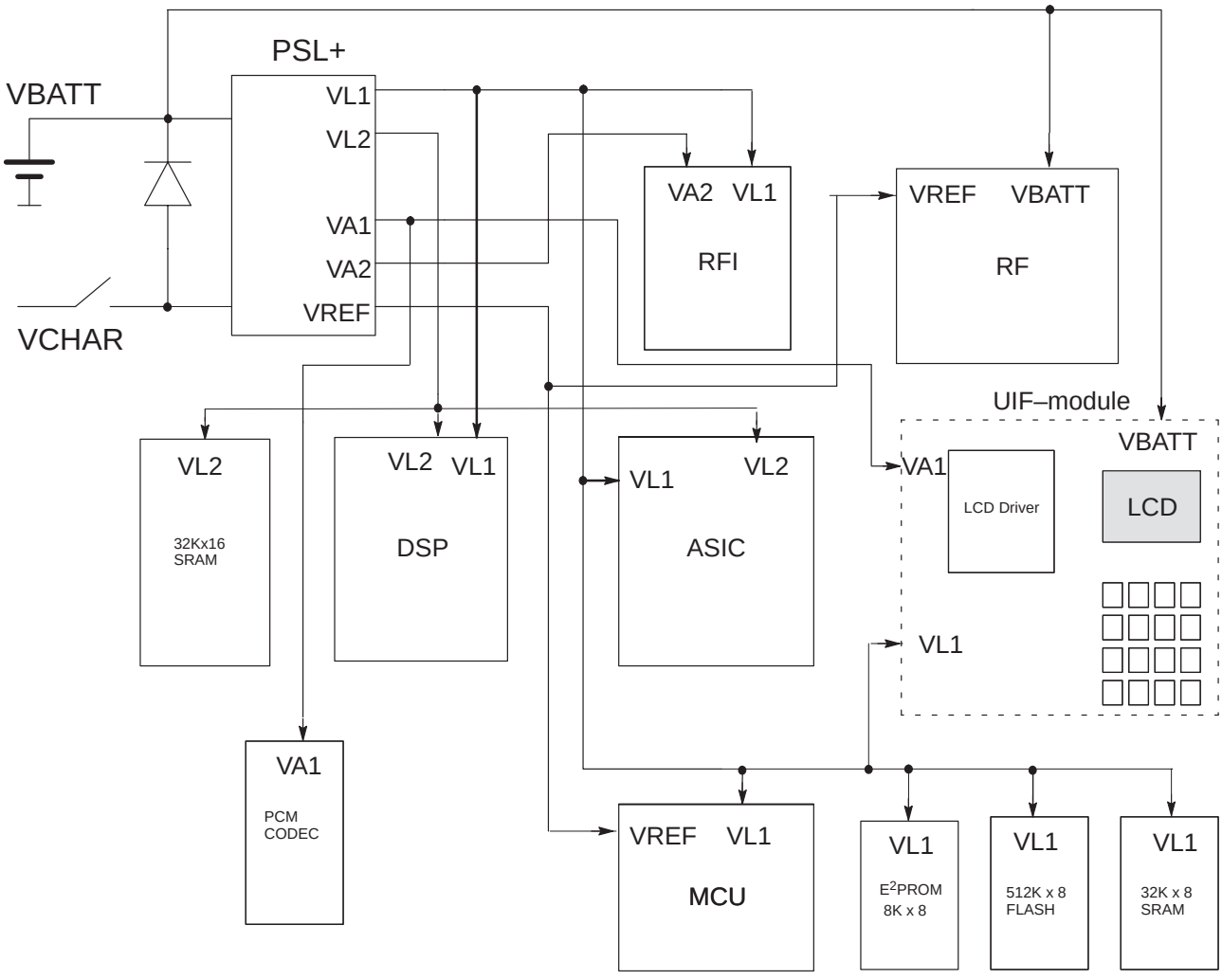
The PLL is PHILIPS UMA1018. The circuit is a dual frequency synthesizer including both the UHF and VHF synthesizers.

Parameter:	*Value*
Supply voltage (min/max):	*2.7...5.5 V*
Supply current (typ):	*8.5 mA*
Principal input frequency (min/max):	*500...1200 MHz, V_{DD} = 4.5 V*
Auxiliary input frequency (min/max):	*20...300 MHz, V_{DD} = 4.5 V*
Input reference frequency (min/max):	*3...40 MHz, V_{DD} = 4.5 V*
Input signal level (min/max):	*50...500 mV_{RMS}*

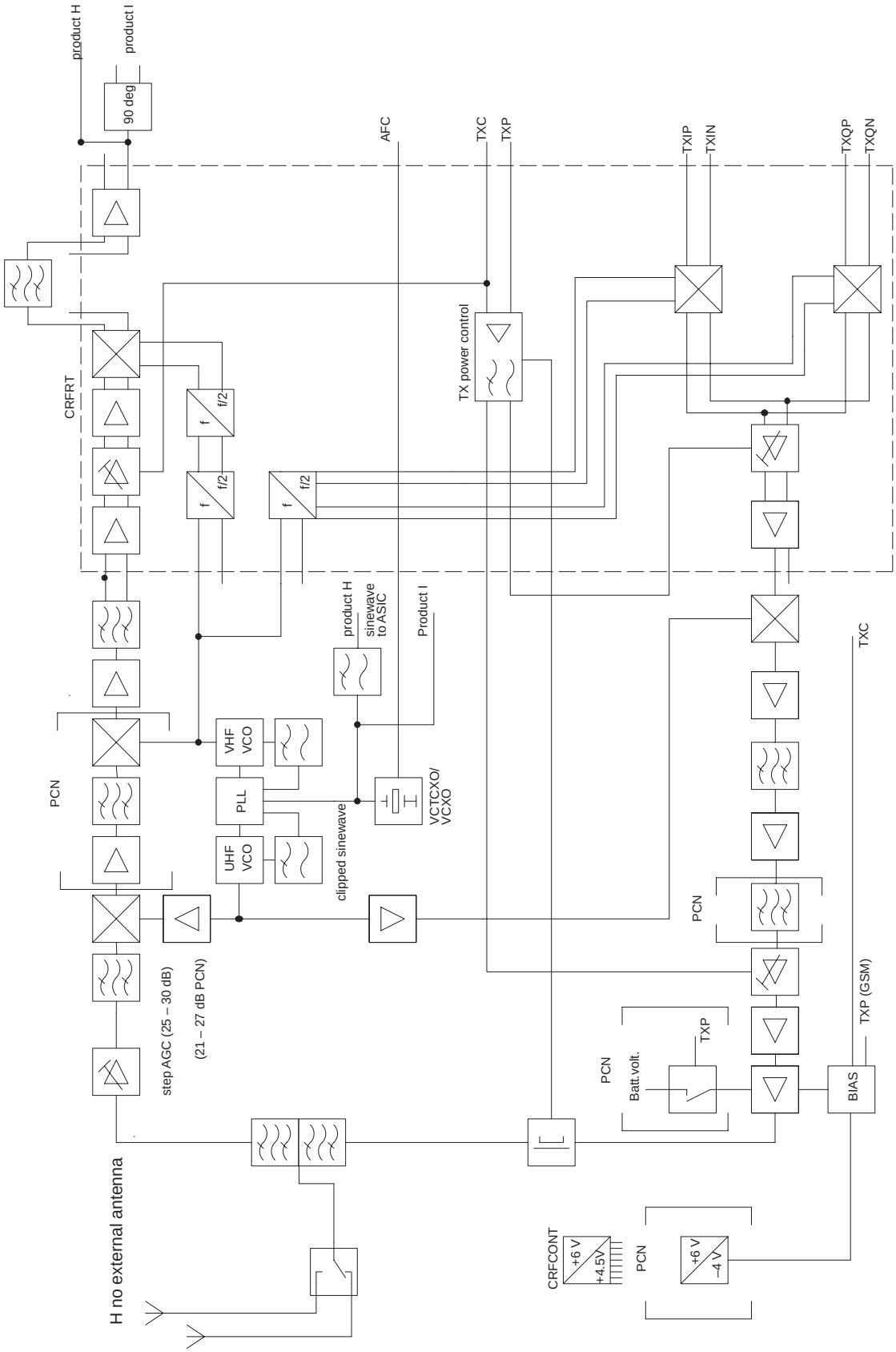
Block Diagram of Baseband



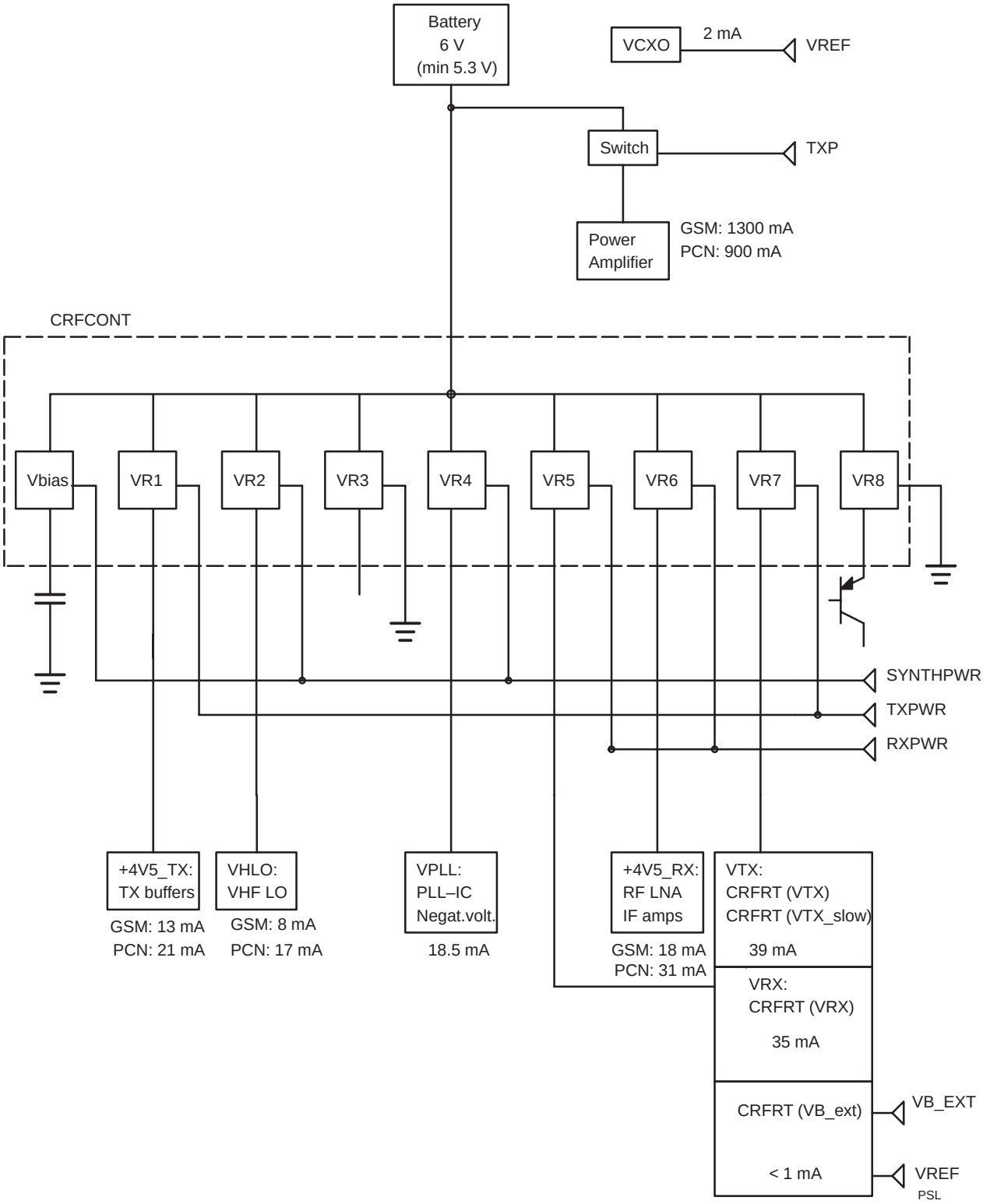
Power Distribution Diagram of Baseband



Block Diagram of RF

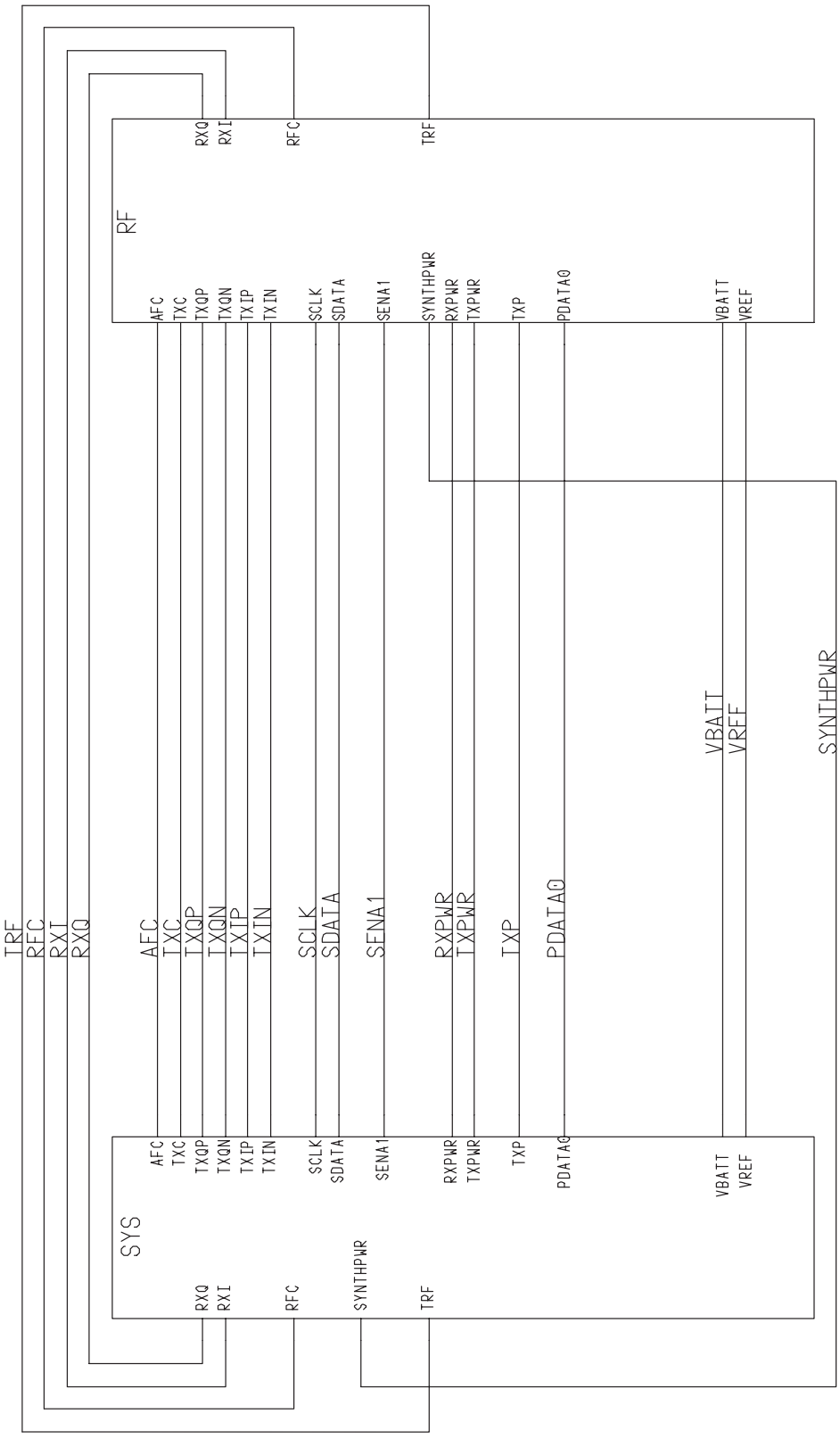


Power Distribution Diagram of RF



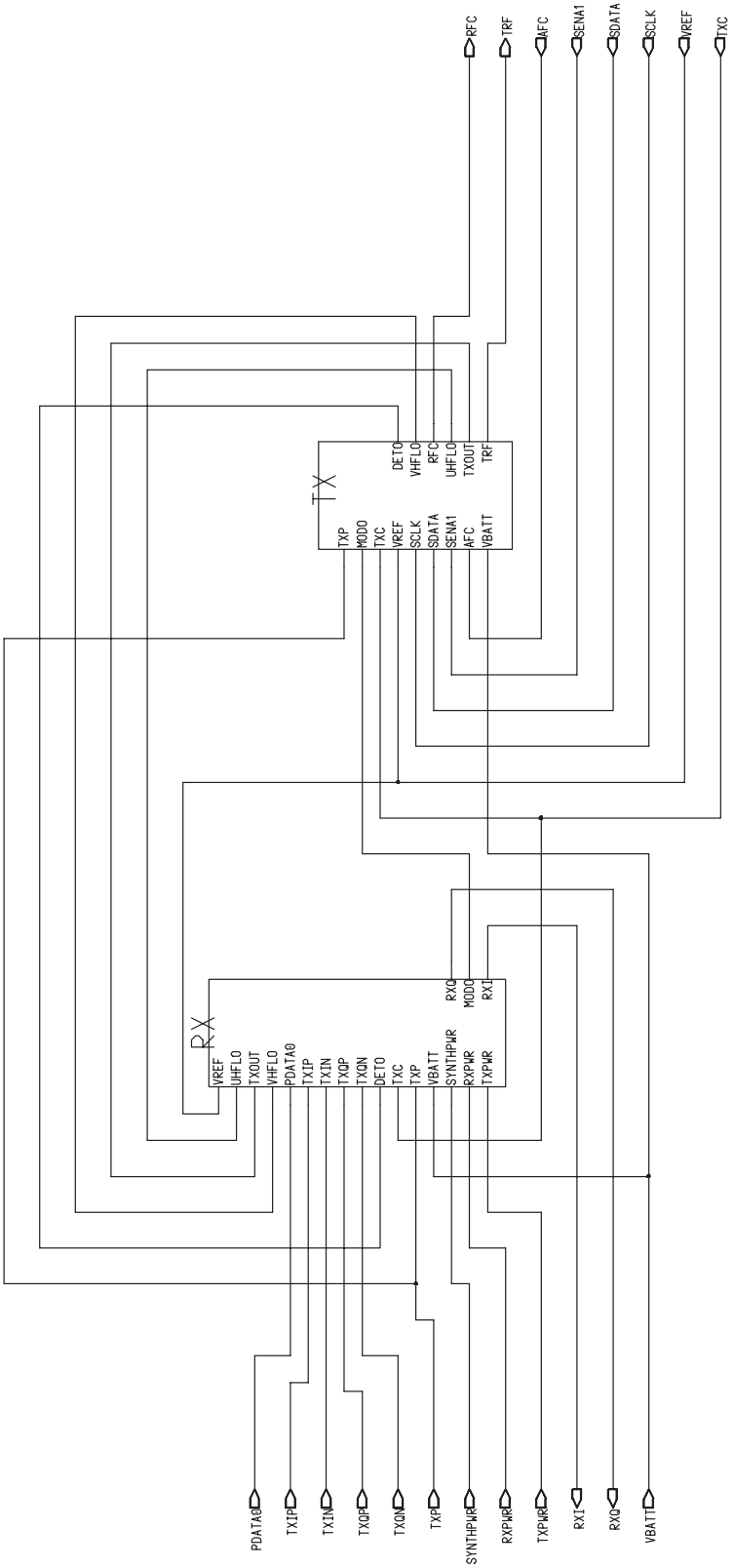
Connections between System and RF Blocks

Version: 5.0 Edit: 111



Connections between RX and TX Blocks

Version: 6.0 Edit: 73



Circuit Diagram of GR8; System Blocks

Circuit Diagram of GR8; CPU & Memories

Circuit Diagram of GR8; Power Supply IC & Batt. Charg. unit

Circuit Diagram of GR8; DSP, Clock Generator & Memories

Circuit Diagram of GR8; Audio Codec IC

Circuit Diagram of GR8; ASIC IC

Circuit Diagram of GR8; RFI IC

Circuit Diagram of GR8; RF Receiver and Regulator

Circuit Diagram of GR8; RF Transmitter

Layout Diagram of GR8 Side 1 Version 09

Layout Diagram of GR8 Side 2 Version 09

Parts List of GR8 (EDMS Issue: 6.8 Code: 0200514)

ITEM	CODE	DESCRIPTION	VALUE	TYPE
R070	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R071	1430794	Chip resistor	39 k	5 % 0.063 W 0402
R072	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R073	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R074	1430730	Chip resistor	150	5 % 0.063 W 0402
R075	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R076	1430744	Chip resistor	470	5 % 0.063 W 0402
R077	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R078	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R079	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R110	1430842	Chip resistor	680 k	1 % 0.063 W 0402
R111	1430840	Chip resistor	220 k	1 % 0.063 W 0402
R112	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R113	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R114	1430732	Chip resistor	180	5 % 0.063 W 0402
R140	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R141	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R142	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R143	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R144	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R145	1430732	Chip resistor	180	5 % 0.063 W 0402
R146	1430846	Chip resistor	2.7 k	1 % 0.063 W 0402
R147	1430844	Chip resistor	3.9 k	1 % 0.063 W 0402
R148	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R149	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R150	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R151	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R152	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R160	1430726	Chip resistor	100	5 % 0.063 W 0402
R161	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R162	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R163	1430726	Chip resistor	100	5 % 0.063 W 0402
R164	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R165	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R166	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R169	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R170	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R171	1430788	Chip resistor	22 k	5 % 0.063 W 0402

R172	1430798	Chip resistor	56 k	5 % 0.063 W 0402
R173	1430794	Chip resistor	39 k	5 % 0.063 W 0402
R174	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R175	1430700	Chip resistor	10	5 % 0.063 W 0402
R176	1430726	Chip resistor	100	5 % 0.063 W 0402
R177	1430726	Chip resistor	100	5 % 0.063 W 0402
R178	1430726	Chip resistor	100	5 % 0.063 W 0402
R179	1430726	Chip resistor	100	5 % 0.063 W 0402
R180	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R181	1430726	Chip resistor	100	5 % 0.063 W 0402
R182	1430726	Chip resistor	100	5 % 0.063 W 0402
R183	1430734	Chip resistor	220	5 % 0.063 W 0402
R184	1430726	Chip resistor	100	5 % 0.063 W 0402
R185	1430726	Chip resistor	100	5 % 0.063 W 0402
R186	1430726	Chip resistor	100	5 % 0.063 W 0402
R190	1430726	Chip resistor	100	5 % 0.063 W 0402
R191	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R192	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R193	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R194	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R195	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R196	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R197	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R198	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R199	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R210	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R230	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R231	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R232	1430842	Chip resistor	680 k	1 % 0.063 W 0402
R233	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R234	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R235	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R236	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R237	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R238	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R239	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R240	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R241	1430744	Chip resistor	470	5 % 0.063 W 0402
R243	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R246	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R247	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R248	1430726	Chip resistor	100	5 % 0.063 W 0402

R249	1430726	Chip resistor	100	5 % 0.063 W 0402
R250	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R251	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R252	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R253	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R254	1430760	Chip resistor	1.8 k	5 % 0.063 W 0402
R255	1430726	Chip resistor	100	5 % 0.063 W 0402
R256	1430726	Chip resistor	100	5 % 0.063 W 0402
R257	1430726	Chip resistor	100	5 % 0.063 W 0402
R260	1430726	Chip resistor	100	5 % 0.063 W 0402
R261	1430784	Chip resistor	15 k	5 % 0.063 W 0402
R262	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R263	1430760	Chip resistor	1.8 k	5 % 0.063 W 0402
R264	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R265	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R267	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R270	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R501	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R502	1430732	Chip resistor	180	5 % 0.063 W 0402
R503	1430732	Chip resistor	180	5 % 0.063 W 0402
R504	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R505	1430772	Chip resistor	5.6 k	5 % 0.063 W 0402
R506	1430710	Chip resistor	22	5 % 0.063 W 0402
R507	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R508	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R509	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R511	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R512	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R513	1430740	Chip resistor	330	5 % 0.063 W 0402
R514	1430710	Chip resistor	22	5 % 0.063 W 0402
R541	1430710	Chip resistor	22	5 % 0.063 W 0402
R542	1430734	Chip resistor	220	5 % 0.063 W 0402
R543	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R544	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R545	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R546	1430724	Chip resistor	82	5 % 0.063 W 0402
R547	1430744	Chip resistor	470	5 % 0.063 W 0402
R551	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R552	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R553	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R554	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R555	1430788	Chip resistor	22 k	5 % 0.063 W 0402

R556	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R557	1430730	Chip resistor	150	5 % 0.063 W 0402
R558	1430732	Chip resistor	180	5 % 0.063 W 0402
R559	1430740	Chip resistor	330	5 % 0.063 W 0402
R560	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R562	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R563	1430728	Chip resistor	120	5 % 0.063 W 0402
R564	1430738	Chip resistor	270	5 % 0.063 W 0402
R565	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R566	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R567	1430728	Chip resistor	120	5 % 0.063 W 0402
R568	1430734	Chip resistor	220	5 % 0.063 W 0402
R569	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R570	1430726	Chip resistor	100	5 % 0.063 W 0402
R571	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R572	1430276	Chip resistor	47 k	2 % 0.063 W 0603
R573	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R574	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R576	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R577	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R578	1430794	Chip resistor	39 k	5 % 0.063 W 0402
R579	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R580	1430790	Chip resistor	27 k	5 % 0.063 W 0402
R583	1430794	Chip resistor	39 k	5 % 0.063 W 0402
R584	1430310	Chip resistor	75 k	2 % 0.063 W 0603
R585	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R586	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R601	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R602	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R603	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R701	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R702	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R703	1430710	Chip resistor	22	5 % 0.063 W 0402
R704	1430740	Chip resistor	330	5 % 0.063 W 0402
R705	1430724	Chip resistor	82	5 % 0.063 W 0402
R708	1430690	Chip jumper		0402
R711	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R712	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R713	1430744	Chip resistor	470	5 % 0.063 W 0402
R714	1430700	Chip resistor	10	5 % 0.063 W 0402
R715	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R716	1430693	Chip resistor	5.6	5 % 0.063 W 0402

R717	1430734	Chip resistor	220	5 % 0.063 W 0402
R725	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R726	1430790	Chip resistor	27 k	5 % 0.063 W 0402
R727	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R728	1430730	Chip resistor	150	5 % 0.063 W 0402
R736	1430786	Chip resistor	18 k	5 % 0.063 W 0402
R737	1430786	Chip resistor	18 k	5 % 0.063 W 0402
R738	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R739	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R740	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R741	1430746	Chip resistor	560	5 % 0.063 W 0402
R742	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R743	1430700	Chip resistor	10	5 % 0.063 W 0402
R755	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R756	1412279	Chip resistor	2.2	5 % 0.1 W 0805
R765	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R766	1430748	Chip resistor	680	5 % 0.063 W 0402
R767	1430732	Chip resistor	180	5 % 0.063 W 0402
R768	1430752	Chip resistor	820	5 % 0.063 W 0402
R769	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R774	1430724	Chip resistor	82	5 % 0.063 W 0402
R775	1430722	Chip resistor	68	5 % 0.063 W 0402
R780	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R781	1430740	Chip resistor	330	5 % 0.063 W 0402
R782	1430726	Chip resistor	100	5 % 0.063 W 0402
R783	1430690	Chip jumper		0402
R784	1430726	Chip resistor	100	5 % 0.063 W 0402
R785	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R800	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R801	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R802	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R803	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R804	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R805	1430786	Chip resistor	18 k	5 % 0.063 W 0402
R806	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R807	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R808	1430734	Chip resistor	220	5 % 0.063 W 0402
R809	1820024	NTC resistor	47 k	5 % 0.2 W 0805
R811	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R820	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R821	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R822	1430798	Chip resistor	56 k	5 % 0.063 W 0402

R823	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R824	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R825	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R826	1430780	Chip resistor	12 k	5 % 0.063 W 0402
R827	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R828	1430786	Chip resistor	18 k	5 % 0.063 W 0402
R829	1430718	Chip resistor	47	5 % 0.063 W 0402
R830	1430718	Chip resistor	47	5 % 0.063 W 0402
R840	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R841	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R842	1430844	Chip resistor	3.9 k	1 % 0.063 W 0402
R843	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R844	1430734	Chip resistor	220	5 % 0.063 W 0402
R845	1430700	Chip resistor	10	5 % 0.063 W 0402
R846	1430726	Chip resistor	100	5 % 0.063 W 0402
R847	1430718	Chip resistor	47	5 % 0.063 W 0402
R860	1430716	Chip resistor	39	5 % 0.063 W 0402
C040	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C041	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C042	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C043	2320598	Ceramic cap.	3.9 n	5 % 50 V 0402
C044	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C045	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C046	2320598	Ceramic cap.	3.9 n	5 % 50 V 0402
C047	2320598	Ceramic cap.	3.9 n	5 % 50 V 0402
C109	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C110	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C111	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C112	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C113	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C114	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C115	2604329	Tantalum cap.	4.7 u	20 % 10 V 3.5x2.8x1.9
C116	2604329	Tantalum cap.	4.7 u	20 % 10 V 3.5x2.8x1.9
C117	2604329	Tantalum cap.	4.7 u	20 % 10 V 3.5x2.8x1.9
C118	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C119	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C120	2604329	Tantalum cap.	4.7 u	20 % 10 V 3.5x2.8x1.9
C121	2604329	Tantalum cap.	4.7 u	20 % 10 V 3.5x2.8x1.9
C122	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C124	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C125	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C126	2320560	Ceramic cap.	100 p	5 % 50 V 0402

C127	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C140	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C141	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C142	2320598	Ceramic cap.	3.9 n	5 % 50 V 0402
C160	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C170	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C171	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C172	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C173	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C175	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C176	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C177	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C178	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C180	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C181	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C182	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C183	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C185	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C186	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C187	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C188	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C195	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C196	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C197	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C198	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C200	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C201	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C202	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C203	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C210	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C211	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C220	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C221	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C230	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C231	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C232	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C233	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C234	2320598	Ceramic cap.	3.9 n	5 % 50 V 0402
C235	2320598	Ceramic cap.	3.9 n	5 % 50 V 0402
C236	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C237	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C239	2320560	Ceramic cap.	100 p	5 % 50 V 0402

C248	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C250	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C251	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C252	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C253	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C255	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C256	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C257	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C258	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C259	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C260	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C261	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C262	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C263	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C264	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C265	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C266	2320598	Ceramic cap.	3.9 n	5 % 50 V 0402
C267	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C268	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C269	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C270	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C271	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C272	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C276	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C277	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C278	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C279	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C282	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C283	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C286	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C287	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C290	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C291	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C296	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C501	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C502	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C503	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C504	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C505	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C506	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C511	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C512	2320550	Ceramic cap.	39 p	5 % 50 V 0402

C513	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C514	2320520	Ceramic cap.	2.2 p	0.25 % 50 V 0402
C515	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C516	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C517	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C521	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C536	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C541	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C542	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C543	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C544	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C545	2320728	Ceramic cap.	220 p	10 % 50 V 0402
C546	2320728	Ceramic cap.	220 p	10 % 50 V 0402
C551	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C552	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C553	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C554	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C555	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C556	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C557	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C558	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C559	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C560	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C561	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C562	2320075	Ceramic cap.	470 p	5 % 50 V 0603
C563	2320578	Ceramic cap.	560 p	5 % 50 V 0402
C564	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C565	2310470	Ceramic cap.	270 p	5 % 50 V 0805
C566	2320558	Ceramic cap.	82 p	5 % 50 V 0402
C567	2310470	Ceramic cap.	270 p	5 % 50 V 0805
C569	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C570	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C571	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C572	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C573	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C574	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C575	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C580	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C601	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C602	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C603	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C604	2310784	Ceramic cap.	100 n	10 % 25 V 0805

C605	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C606	2310752	Ceramic cap.	10 n	20 % 50 V 0805
C607	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C608	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C609	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C701	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C702	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C703	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C704	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C705	2320520	Ceramic cap.	2.2 p	0.25 % 50 V 0402
C710	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C711	2320558	Ceramic cap.	82 p	5 % 50 V 0402
C712	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C713	2320516	Ceramic cap.	1.5 p	0.25 % 50 V 0402
C716	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C720	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C721	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C722	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C723	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C725	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C726	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C728	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C730	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C731	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C732	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C735	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C736	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C737	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C738	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C739	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C740	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C741	2320556	Ceramic cap.	68 p	5 % 50 V 0402
C742	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C743	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C744	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C755	2320556	Ceramic cap.	68 p	5 % 50 V 0402
C756	2320578	Ceramic cap.	560 p	5 % 50 V 0402
C757	2320578	Ceramic cap.	560 p	5 % 50 V 0402
C758	2320556	Ceramic cap.	68 p	5 % 50 V 0402
C759	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C760	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C761	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402

C762	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C763	2500708	Electrol. cap.	3300 u	20 % 16 V
C764	2320361	Ceramic cap.	18 p	2 % 25 V 0603
C768	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C780	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C781	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C782	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C783	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C784	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C800	2604079	Tantalum cap.	0.22 u	20 % 35 V 3.2x1.6x1.6
C801	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C803	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C804	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C805	2320728	Ceramic cap.	220 p	10 % 50 V 0402
C806	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C807	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C808	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C809	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C810	2320728	Ceramic cap.	220 p	10 % 50 V 0402
C820	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C821	2310167	Ceramic cap.	1.0 n	5 % 50 V 1206
C822	2320053	Ceramic cap.	56 p	5 % 50 V 0603
C823	2310248	Ceramic cap.	4.7 n	5 % 50 V 1206
C824	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C828	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C829	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C830	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C831	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C832	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C840	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C841	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C842	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C843	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C844	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C845	2320604	Ceramic cap.	18 p	5 % 50 V 0402
C846	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C847	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C848	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C849	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C850	2320604	Ceramic cap.	18 p	5 % 50 V 0402
C851	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C862	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402

C863	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402	
L004	3641302	Chip coil 470 n	5 % Q=30/25 MHz 1008		
L140	3606946	Ferrite bead 0.2r 26r/100mhz 1206			1206
L180	3606946	Ferrite bead 0.2r 26r/100mhz 1206			1206
L270	3641262	Ferrite bead 30r/100mhz 2a 1206			1206
L271	3641262	Ferrite bead 30r/100mhz 2a 1206			1206
L272	3606946	Ferrite bead 0.2r 26r/100mhz 1206			1206
L273	3606946	Ferrite bead 0.2r 26r/100mhz 1206			1206
L511	3641550	Chip coil 120 n	10 % Q=35/150 MHz 0805		
L532	3641550	Chip coil 120 n	10 % Q=35/150 MHz 0805		
L541	3641550	Chip coil 120 n	10 % Q=35/150 MHz 0805		
L542	3608326	Chip coil 330 n	5 % Q=33/50 MHz 1206		
L543	3641560	Chip coil 220 n	10 % Q=30/100 MHz 0805		
L544	3641560	Chip coil 220 n	10 % Q=30/100 MHz 0805		
L545	3608326	Chip coil 330 n	5 % Q=33/50 MHz 1206		
L546	3608326	Chip coil 330 n	5 % Q=33/50 MHz 1206		
L551	3641538	Chip coil 39 n	20 % Q=40/250 MHz 0805		
L700	3606946	Ferrite bead 0.2r 26r/100mhz 1206			1206
L705	3640013	Chip coil 8 n	5 % Q=50/250 MHz 0805		
L710	3641626	Chip coil 220 n	2 % Q=30/100 MHz 0805		
L711	3641542	Chip coil 56 n	10 % Q=40/200 MHz 0805		
L800	3641206	Chip coil	10 % Q=25/7.96 MHz 1008		
L801	3641206	Chip coil	10 % Q=25/7.96 MHz 1008		
L840	3641574	Chip coil 68 n	5 % Q=40/200 MHz 0805		
L841	3641538	Chip coil 39 n	20 % Q=40/250 MHz 0805		
B001	4510044	Crystal 60.2 M			
B800	4510071	Crystal 26.000 M			
G001	4352933	Vco 1006–1031mhz4.5v 15ma dct2gsm			DCT2GSM
Z500	4512046	Dupl 890–915/935–960mhz 37x14.7			37x14.7
Z505	4511016	Saw filter 947.5+–12.5 M	5.4x5.2		
Z541	4511026	Saw filter 71+–0.08 M	14.2x8.4		
Z551	4556998	Cer.filt 13+–0.22mhz 330r 7x3rad			7x3rad
Z713	4550101	Cer.filt 902.5+–12.5mhz 9.4x8.9			9.4x8.9
T070	3640402	Transformer 4:1 balun 800mhz smd			SMD
V110	4210020	Transistor	BCP69–25	pnp 20 V 1 A SOT223	
V111	4200877	Transistor	BCX51–16	pnp 45 V 1.5 A SOT89	
V141	4113828	Trans. supr.	SMBJ28A	DO214AA	
V142	4210020	Transistor	BCP69–25	pnp 20 V 1 A SOT223	
V143	4200226	Darl. transistor	BCV27	npn 30 V 300 mA SOT23	
V144	4200226	Darl. transistor	BCV27	npn 30 V 300 mA SOT23	
V145	4200909	Transistor	BC858B/BCW30	pnp 30 V 100 mA SOT23	
V147	4110126	Zener diode	BZX84	5 % 4.3 V 0.3 W SOT23	

V148	4110074	Schottky diode	STPS340U	40 V 3 A SOD6	
V160	4210100	Transistor	BC848W	npn 30 V SOT323	
V161	4210100	Transistor	BC848W	npn 30 V SOT323	
V210	4110014	Sch. diode x 2	BAS70–07	70 V 15 mA SOT143	
V214	4210079	Transistor	SOT23		
V215	4210079	Transistor	SOT23		
V216	4210050	Transistor	DTA114EE	pnp RB V EM3	
V219	4210100	Transistor	BC848W	npn 30 V SOT323	
V250	4210100	Transistor	BC848W	npn 30 V SOT323	
V251	4200909	Transistor	BC858B/BCW30	pnp 30 V 100 mA SOT23	
V252	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MWSOT323	
V270	4117998	Precision voltage reference	4.096	4.096	
V501	4210046	Transistor	BFP182	npn 20 V 35 mA SOT143	
V502	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MWSOT323	
V503	4210100	Transistor	BC848W	npn 30 V SOT323	
V511	4115802	Sch. diode x 2	4V	30 mA SOT23	
V512	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323	
V541	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323	
V701	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323	
V702	4100567	Sch. diode x 2	BAS70–04	70V15 mA SERSOT23	
V710	4200755	Transistor	BFR92A	npn 15 V 25 mA SOT23	
V725	4200755	Transistor	BFR92A	npn 15 V 25 mA SOT23	
V726	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MWSOT323	
V735	4210100	Transistor	BC848W	npn 30 V SOT323	
V736	4217070	Transistor x 2		IMD	
V737	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MWSOT323	
V738	4210090	Transistor	BFG540/X	npn 15 V 129 mA SOT143	
V755	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MWSOT323	
V756	4210133	Transistor	BFG10W/X	npn 10 V 0.25 A SOT343	
V765	4210100	Transistor	BC848W	npn 30 V SOT323	
V766	4210100	Transistor	BC848W	npn 30 V SOT323	
V767	4100285	Diode x 2	BAV99	70 V 200 mA SER.SOT23	
V768	4210135	Transistor	BLT82	npn 10 V SO8S	
V780	4110014	Sch. diode x 2	BAS70–07	70 V 15 mA SOT143	
V800	4110081	Cap. diode	BB640	28/1 V SOD323	
V801	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323	
V802	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323	
V840	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323	
V841	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323	
V842	4110018	Cap. diode	BB135	30 V SOD323	
D181	4346010	IC, SRAM	32kx8 bit 70 ns TSOP28		
D184	4342282	M28c6	4C150 EEPROM 8KX8 150NSTSO2150NSTSO28		

D185	4340201	IC, flash memory	E28F008	TSO40	
D191	4340126	IC, 1xnand 2input cmos	ss	TC7S00F	SSO5
D192	4340126	IC, 1xnand 2input cmos	ss	TC7S00F	SSO5
D200	4372231	IC, ROM	DSP1616S11	TQFP100	
D210	4346012	IC, SRAM	32kx8 bit 70 ns	TSO28	
D211	4346010	IC, SRAM	32kx8 bit 70 ns	TSOP28	
D230	4370092	IC, D2CA GSM/PCN ASIC		SQFP144	
D231	4375174	IC, MCU	SQFP80		
N260	4343132	IC, PCM coded/filter	ST5080	SO28W	
N270	4370015	IC, ASIC	SQFP64		
N271	4375588	IC, PSL+ power supply		SO24W	
N551	4370091	Crfrt_st tx.mod+rxif+pwc	sqfp44		SQFP44
N601	4370095	Crfcontf 8xreg4.5v vref2v5	vsop28		VSOP28
N820	4340069	IC, 2xsynt 3v sso	UMA1018M/C1/C3/S1		SSO20
X100	5469033	System conn	4DC+JACK+16AF+1RF		
X196	5431718	Flexfoil connect 1x30 0.5mm smd			
X501	9510143	Antenna clip	4D23053	NHK–1XA	
W501	9780074	Coax cable	4D23278	NHK–1XA	
	9380233	Sticker brady lat–11–747w–5			
	9480204	Damping pad	4D25528	NHE–4	
	9854011	PCB GR8 50.0X139.0X1.0 M6 2/PA			